Advanced Engineering Technology and Application
An International Journal

http://dx.doi.org/10.18576/aeta/050101

Design of Delay-Power Efficient Carry Select Adder using 3-T XOR Gate

Gagandeep Singh Gill[1,*] *and Navjot Kaur*[2]

[1] ECE Department Shaheed Bhagat Singh State Technical Campus Ferozepur, Punjab, India
[2] CSE Department Shaheed Bhagat Singh State Technical Campus Ferozepur, Punjab, India

Received: 14 Jun. 2015, Revised: 8 Oct. 2015, Accepted: 27 Oct. 2015
Published online: 1 Jan. 2016

Abstract: In VLSI system design, the digital adders significantly affects the overall proficiency of the system. Having adders with low cost and fast addition operation is the most desirable requirement in todays VLSI design and Carry Select Adder (CSLA) is the most appropriate among all known adder structures. This proposed work uses a 3T XOR gate to design a 16-bit CSLA which largely reduces the total transistor count of 16-bit CSLA as XOR gates are essential block in adders. This reduction in total transistor count helps in the reduction of power consumption and power-delay product (PDP) with an increase in speed when compared with Modified-CSLA.

Keywords: Carry Select Adder (CSLA), power, delay, PDP, 3-T XOR gate, MOSFET

1 Introduction

The growing market of portable equipments like cellular phones and laptops demands the microelectronic circuits design with ultra low power dissipation. As the integration, size and complexity of chips continue to increase, there is a significant increase in power consumption [1,2,3,4]. As adders are basic building blocks of complex arithmetic circuits, therefore any optimization of their speed and power consumption can have considerable impact on power efficiency and speed of the overall system. Adders are widely used in Central Processing Unit (CPU), Arithmetic Logic Unit (ALU) and floating point units, for address generation in case of cache or memory access and in digital signal processing [5,6].

Addition is the most basic arithmetic operation. For adding two binary numbers several adder structures based on very different design ideas exist. Thus to implement an addition circuit one must decide which circuit is most appropriate for its planned application. Depending upon the area, delay, and power consumption, the various adders are categorized as ripple carry adder (RCA), carry select adder (CSLA) and carry look ahead adder (CLAA). CSLA provides a balance between the small area but longer delay of RCA and the large area with small delay of CLAA [7]. In CSLA, pair of RCAs are used for addition, that is, one block of RCA with Cin (carry in) = 0 and other block of RCA with Cin = 1. Depending on the value of previous carry, the final sum and carry outputs are selected using multiplexer. As the pair of RCAs used for each bit addition increases the complexity as well as transistor count, the simplest kind of CSLA is not very efficient [8].

As well known, XOR gates form the fundamental building block of full adders, therefore enhancing the performance of the XOR gates can significantly improve the performance of the adder. In our previous work, 3T XOR gate based 8-bit CSLA was designed which showed the enhancement in the performance of 8-bit CSLA in terms of power consumption and power delay product [9]. Here in this paper, we have extended our work to design a 16-bit CSLA using 3T-XOR gate based on static CMOS inverter logic and Pass transistor logic (PTL). The main advantage of using 3T-XOR gate is that the power consumption as well as the delay time of the circuit decreases due to the large decrease in number of switching transistors (MOSFETs) used in the design of 16-bit CSLA.

This paper is organized as follows. Section 2 shows the previous works done on carry select adder including the detailed structure and analysis of Regular CSLA as well as Modified CSLA. Section 3 explains the proposed

* Corresponding author e-mail: gagan.gill010@gmail.com

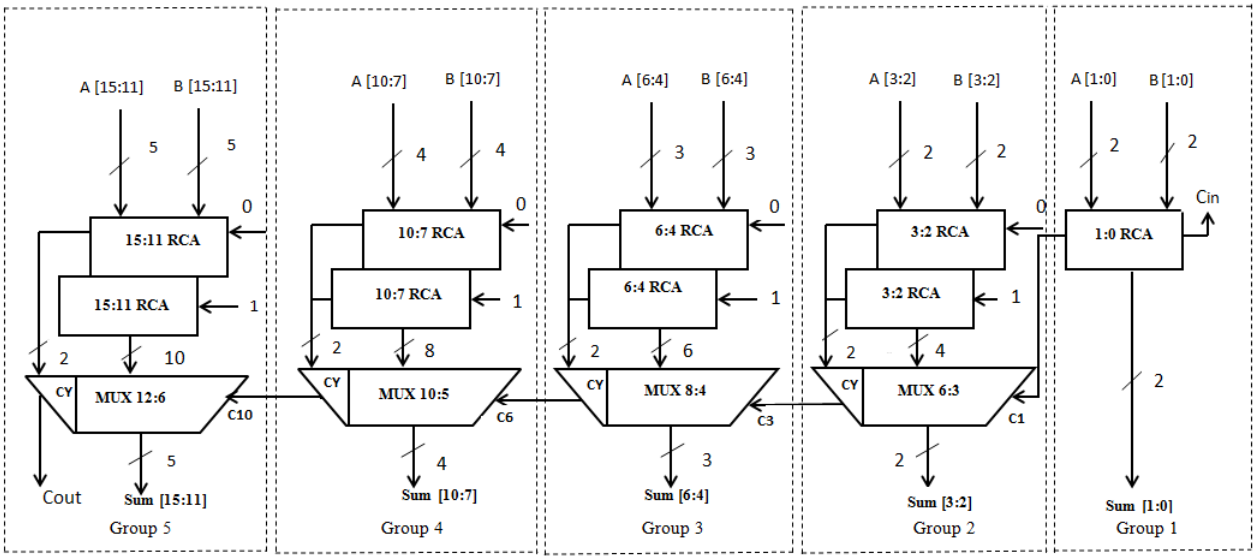


Fig. 1: Regular 16-bit CSLA.

Table 1: Truth table of 4-bit BEC

I[3:0]	X[3:0]
0000	0001
0001	0010
0010	0011
0011	0100
0100	0101
0101	0110
0110	0111
0111	1000
1000	1001
1001	1010
1010	1011
1011	1100
1100	1101
1101	1110
1110	1111
1111	0000

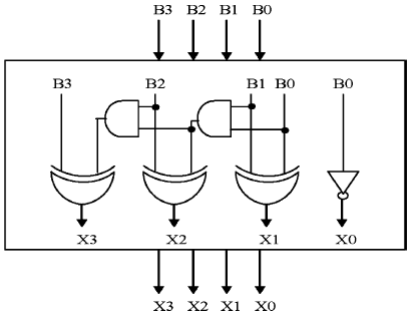


Fig. 2: 4-bit BEC circuit.

CSLA and evaluates the reduction in switching transistors (MOSFETs) count. The implementation details as well as simulation results of proposed CSLA are analyzed in Section 4 and Section 5 concludes the whole work.

2 PREVIOUS WORKS ON CARRY SELECT ADDER

In digital adder circuits, the sum output for each bit position is produced sequentially only after the previous bit position has been summed and a carry propagated into the next position. Therefore the speed of addition (delay time) is limited due to the time taken by the carry signal to propagate through the adder. The introduction of Regular carry select adder (R-CSLA) mitigated the problem of carry propagation delay as multiple carries are generated independently and the correct sum and carry outputs are selected depending on the value of previous carry [8]. As discussed earlier, this type of CSLA (i.e., R-CSLA) was not area as well as power efficient due to the use of pair of RCAs (each for Cin = 0 and Cin = 1) to produce the final sum and carry output. The 16-bit R-CSLA is shown in Figure 1.

As the use of pair of RCA's largely degrades the performance of R-CSLA, various attempts have been made to avoid the dual use of RCA in CSLA design [10, 11]. To overcome this problem of dual RCA's, an add-one circuit known as Binary to Excess-1 Converter (BEC)

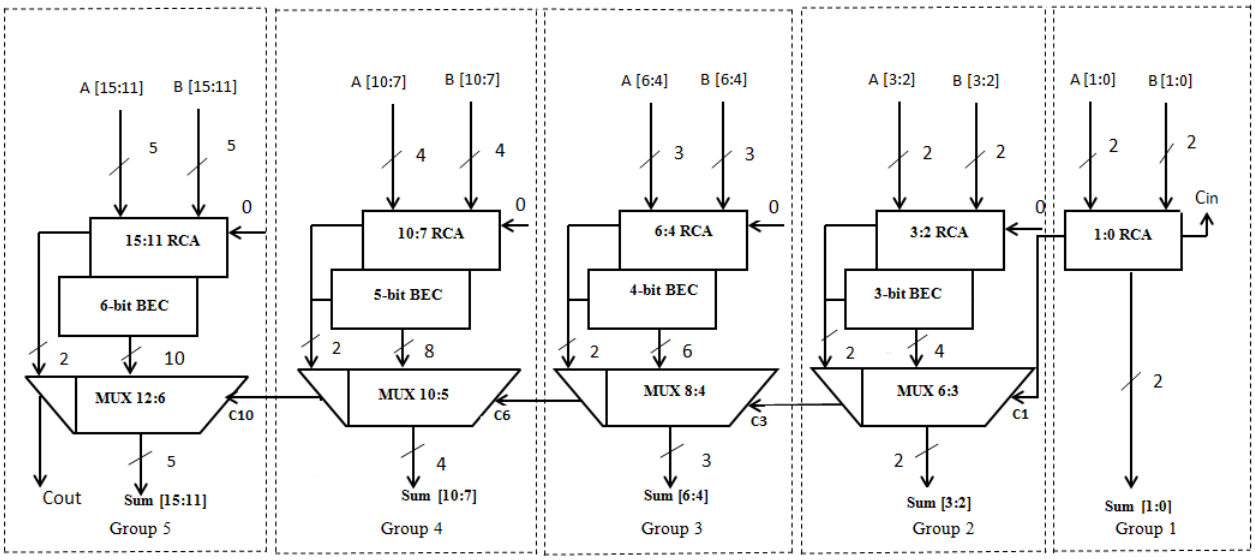


Fig. 3: Modified 16-bit CSLA.

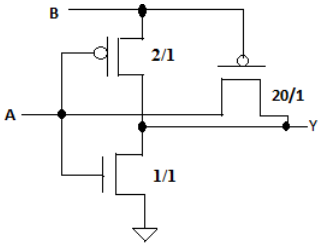


Fig. 4: 3-T XOR gate.

circuit was introduced. BEC is a circuit which simply adds 1 to the input bits. This BEC circuit replaced the RCA with Cin = 1 used in R-CSLA which results in low power consumption and an area efficient CSLA as lesser numbers of logic gates were used in BEC as compared to n-bit RCA [12,13]. The circuit diagram and truth table of 4-bit BEC are shown in Figure 2 and Table 1, respectively.

The 16-bit modified carry select adder (M-CSLA) having modified area and power consumption due to the use of BEC (add-one circuit) is shown in Figure 3. As shown in the Figure 3, 16-bit M-CSLA was divided into five groups with different bit sizes of RCA and BEC. This M-CSLA contains different bit sized RCAs (for Cin = 0), BEC circuits (for Cin = 1), and multiplexers (MUX). One input to the MUX is sum along with carry outputs from RCA and another input to the MUX is sum along with carry outputs from BEC circuit. The final correct sum and carry outputs are selected depending upon the value of previous carry which is inputted as a select line to the MUX. As the BEC circuit uses lesser number of logic gates (or transistors) than the RCA, the M-CSLA has reduced area and power consumption with small speed penalty as compared to R-CSLA but there is still scope to enhance the performance of M-CSLA [12].

Table 2: Comparison of various Carry Select Adders

Adder	Total Power (μW)	Delay (ns)	Power-Delay Product (10^{-15})
16- bit Regular CSLA [8]	527.5	2.775	1463.8
16- bit Modified CSLA [12]	471.8	3.048	1438
16- bit CSLA [15]	453.6	3.025	1372
16- bit Proposed CSLA	273.4	2.555	697.17

3 PROPOSED WORK ON CSLA

The XOR gates form the basic building block of CSLA, therefore any modification in XOR gate can largely enhance the performance of CSLA. This proposed work simply focuses on a modified XOR gate. Here, we use a 3-T XOR gate instead of 12-T XOR gate used in previous designs of Regular-CSLA and Modified-CSLA which helps in reduction in transistor count and enhancing various performance parameters of CSLA like power consumption, delay time and Power-Delay Product (PDP) [14]. The circuit diagrams of 3-T XOR gate and proposed 16-bit CSLA are shown in Fig. 4 and Fig. 5 respectively.

A single modified XOR gate (3-T XOR gate) used in this work has 9 lesser transistors as compared to the XOR gate (12-T XOR gate) used in earlier works on CSLA. The proposed 16-bit CSLA is divided into 5 groups as shown in Fig.5. The total reduction in transistor count for

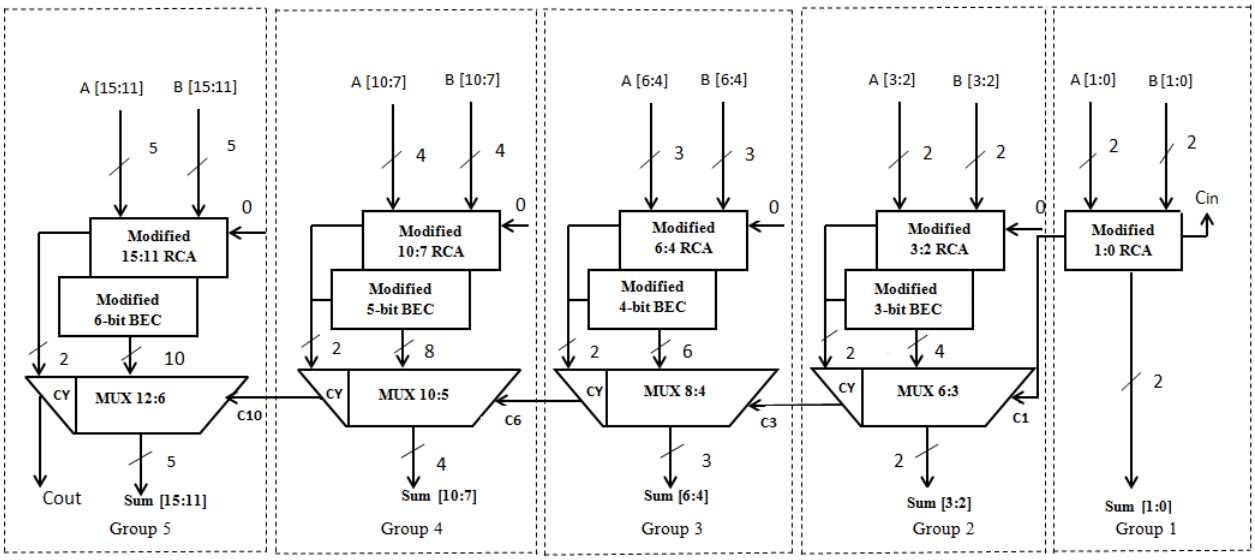
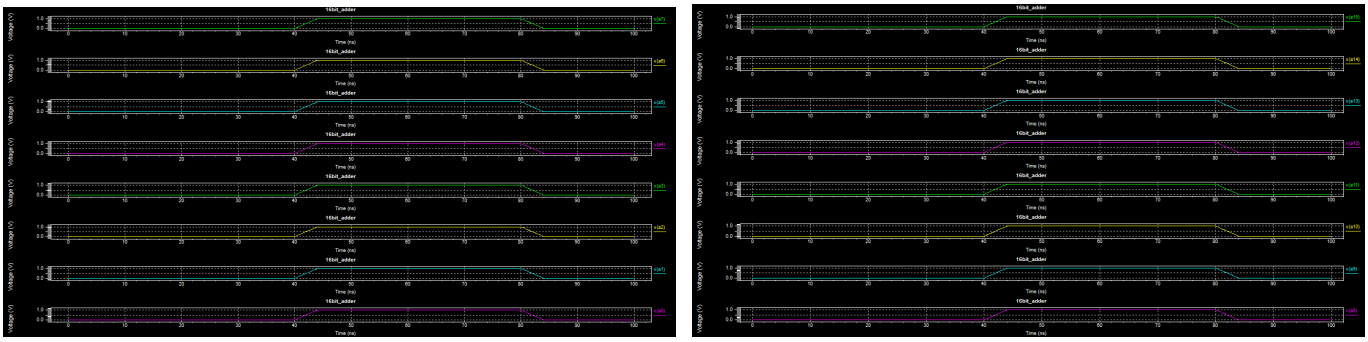
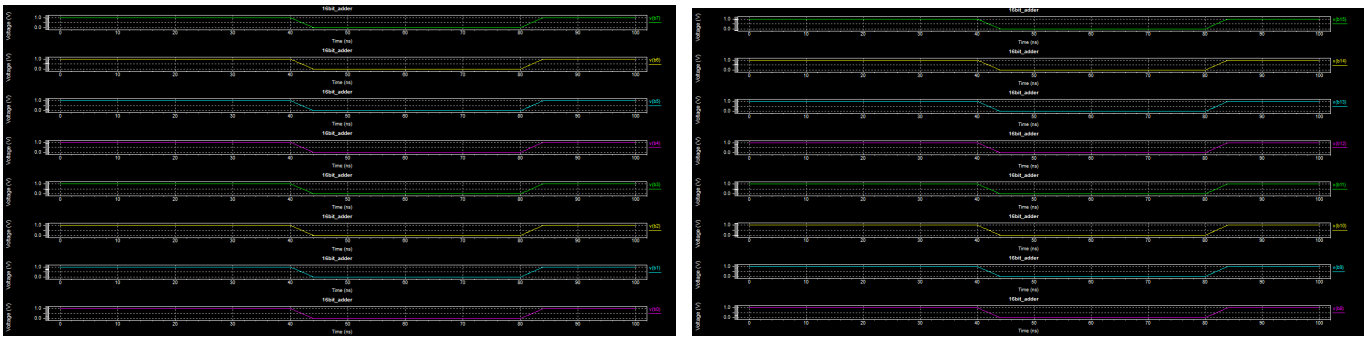


Fig. 5: Proposed 16-bit CSLA.



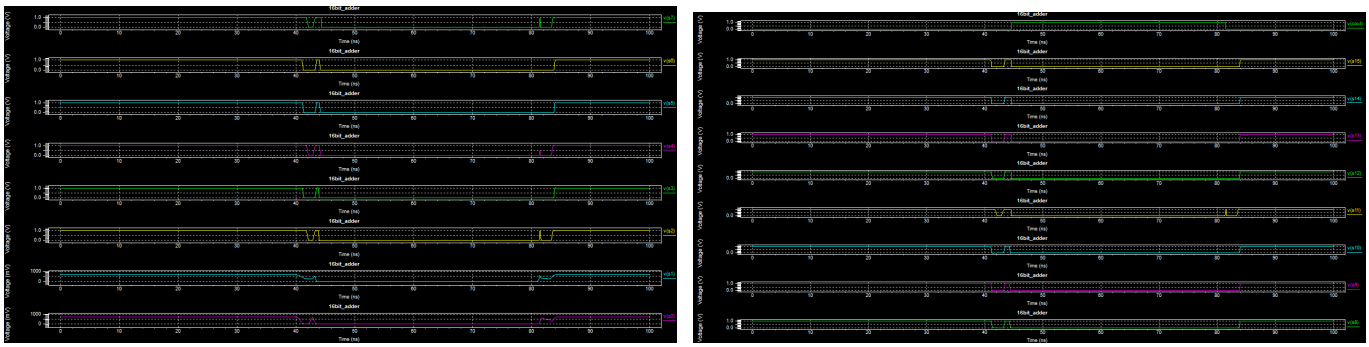
(a) (b)

Fig. 6: Post simulation results: (a) input waveform A0 to A7 and (b) input waveform A8 to A15



(a) (b)

Fig. 7: Post simulation results: (a) input waveform B0 to B7 and (b) input waveform B8 to B15



(a) (b)

Fig. 8: Post simulation results: (a) output waveform S0 to S7 and (b) output waveform S8 to S15 and C_out.

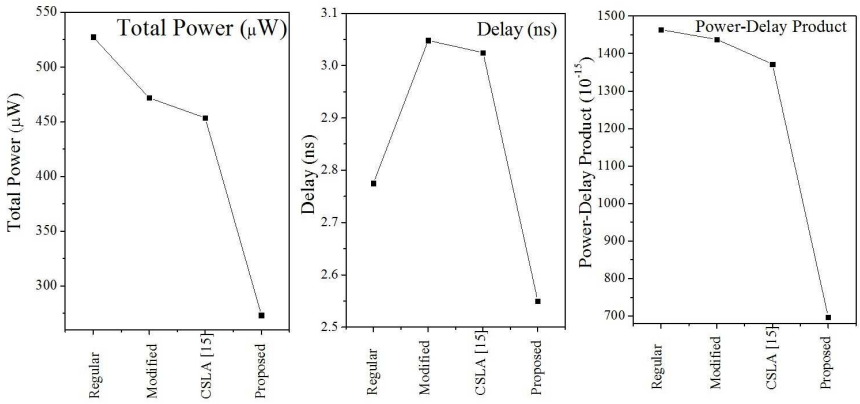


Fig. 9: Power, Delay and PDP comparison for various CSLAs

each group is calculated below:-

Group1-It contains two Full adders. As each full adder consists of two XOR gates, therefore total transistor count reduction for group 1 is:-

Number of XOR gates used = 4

Transistor count reduction = 36 (4*9).

Group2-It contains one Full adder, one Half adder and one 3-bit Binary to Excess-1 Converter (BEC). The transistor count reduction for group 2 is as follows:

Number of XOR gates used = 5 (2+1+2)

Transistor count reduction = 45 (5*9).

Group3-It contains two Full adders, one Half adder and one 4-bit Binary to Excess-1 Converter (BEC). The transistor count reduction for group 3 is as follows:-

Number of XOR gates used = 8 (2*2) +1+3

Transistor count reduction = 72 (8*9).

Group4-It contains three Full adders, one Half adder and one 5-bit BEC. The transistor count reduction for group 4 is as follows:-

Number of XOR gates used = 11 (3*2) +1+4

Transistor count reduction = 99 (11*9).

Group5-It contains four Full adders, one Half adder and one 6-bit BEC. The transistor count reduction for group 5 is as follows:-

Number of XOR gates used = 14 (4*2) +1+5

Transistor count reduction = 126 (14*9).

On adding up the transistor count reduction for all the five groups, the overall reduction in number of switching transistors (MOSFET's) in proposed 16-bit CSLA as compared to the previously designed 16-bit M-CSLA is 378. This large reduction in number of switching transistors due to the use of 3-T XOR gate reduces the power consumption, delay time as well as the Power-delay product (PDP) of 16-bit CSLA.

4 SIMULATION RESULTS

The proposed design of 16-bit CSLA has been simulated in Tanner Tools version 13.0 using 90 nm technology having an input supply voltage of 1.0 V. The proposed design is simulated with a 12.5MHz waveform with rise and fall times of 4 ns. In this design, the power-delay simulation of the proposed 16-bit CSLA has been carried out for all input patterns and from the simulation results, the worst case power consumption as well as delay time is noted down. The power consumption, delay time and

Power-delay product (PDP) of proposed 16-bit CSLA is compared with 16-bit R-CSLA and M-CSLA. The comparison is shown in Table 2

It is evident from the table that the proposed 16-bit CSLA has the superior performance as compared to all other existing CSLA's. The power consumption of proposed CSLA is significantly reduced when compared with M-CSLA and R-CSLA. The attractive feature of proposed 16-bit CSLA is that instead of any speed penalty with reduction in power consumption, the new designed CSLA has reduced delay time which was not achieved in earlier designs. The proposed 16-bit CSLA has power consumption reduction by 48.2% and 42.1% and delay time reduction by 8.1% and 16.3% when compared with R-CSLA and M-CSLA respectively. The Power-delay product (PDP) of proposed 16-bit CSLA is greatly reduced by 52.3% and 51.5% when compared with R-CSLA and M-CSLA respectively. The proposed CSLA also performs much better than other CSLA's present in literature [15].

The post simulation input-output waveforms for the 16-bit proposed CSLA are shown in Figures 6, 7 and 8, respectively. Figure 9 shows the comparison of various carry select adders in graphical form for the data given in Table II. As shown in the graph the proposed CSLA has the best performance in terms of power consumption, delay time and Power-delay product (PDP) when compared with regular CSLA [8], modified CSLA [12], CSLA [15].

5 CONCLUSION

Knowing that the performance of CSLA largely depends upon the XOR gate used, here in this work a 16-bit CSLA is designed using a 3T XOR gate instead of 12T XOR gate which results in large reduction in number of switching transistors (MOSFETs). The attractive feature of proposed 16-bit CSLA is that instead of any increase in delay time (speed penalty) with the reduction in power consumption, the Proposed 16-bit CSLA has decreased delay time. When compared with other existing CSLA's like R- CSLA and M-CSLA, the proposed 16-bit CSLA has reduction in power consumption by 48.2% and 42.1% and delay time reduction by 8.1% and 16.3% respectively. Therefore the power-delay product (PDP) is reduced by 52.3% and 51.5% when compared with R-CSLA and P-CSLA respectively. Therefore the proposed 16-bit CSLA is a very good option for low power, high speed circuit design. In future it would be interesting to design 32-bit and 64-bit CSLA using 3T XOR gate.

References

[1] K. Navi, M. H. Moaiyeri, R. F. Mirzaee, O. Hashemipour, and B. M. Nezhad, "Two new low-power Full Adders based on majority-not gates",*Microelectronics Journal*, vol. 40, no. 1, pp. 126-130, 2009.

[2] Wang, M. F. Yang, W. Cheng, X. G. Guan, Z. M. Zhu, and Y. T. Yang, "Novel low power full adder cells in 180 nm CMOS technology," in *Proceedings of the 4th IEEE Conference on Industrial Electronics and Applications (ICIEA '09)*, pp. 430-433, Xi'an, China, May 2009.

[3] N. Weste and K. Eshraghian,*Principles of CMOS VLSI Design: A Systems Perspective*,Addison-Wesley, Reading, Mass, USA, 1993.

[4] S. Kang and Y. Leblebici,*CMOS Digital Integrated Circuit Analysis and Design*,McGraw-Hill, New York, NY, USA, 3rd edition, 2005.

[5] J. M. Rabaey, A. Chandrakasan, and B. Nikolic, *Digital Integrated Circuits, A Design Perspective*,Prentice Hall, Englewood Cliffs, NJ, USA, 2nd edition, 2002.

[6] J. Uyemura, "CMOS Logic Circuit Design," Kluwer Academic Publishers, New York, NY, USA, 1999.

[7] K. Rawat, T. Darwish, and M. Bayoumi, "A low power and reduced area carry select adder," in *Proceedings of the 45th Midwest Symposium on Circuits and Systems*,pp. I467-I470,August 2002.

[8] O. J. Badrij, "Carry-select Adder,"*IRE Transactions on Electronics Computers*,pp. 340-344, 1962

[9] Gagandeep Singh, and Chakshu Goel. "Design of Low Power and Efficient Carry Select Adder Using 3-T XOR Gate." Advances in Electronics 2014 (2014).

[10] Y. Kim and L.S. Kim, "64-bit carry-select adder with reduced area,"*Electron. Lett.*,vol. 37, no. 10, pp. 614-615, May 2001.

[11] Y. He, C. H. Chang, and J. Gu, "An area-efficient 64-bit square root carry select adder for low power application," in *Proc. IEEE Int. Symp. Circuits Syst., 2005*,vol. 4, pp. 4082-4085.

[12] B. Ramkumar and H. M. Kittur, "Low-power and area-efficient carry select adder," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*,vol. 20, no. 2, pp. 371-375, 2012.

[13] T.-Y. Chang and M.-J. Hsiao, "Carry-select adder using single ripple-carry adder,"*Electronics Letters*, vol. 34, no. 22, pp. 2101-2103, 1998.

[14] S. R. Chowdhury, A. Banerjee, A. Roy, and H. Saha, "A high speed 8 transistor full adder design using novel 3 transistor XOR gates," *International Journal of Electronics, Circuits and Systems*, vol. 2, no. 4, pp. 217-223, 2008.

[15] Sarabdeep Singh, Dilip Kumar, Design of Area and Power Efficient Modified Carry Select Adder, International Journal of Computer Applications, vol.33, no.3, pp.14-18,Nov 2011.