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A Fast-Locking Digital Delay-Locked Loop with Multiphase Outputs using Mixed-Mode-Controlled Delay Line

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Abstract: This paper proposes a fast-locking digital delay-locked loop (DLL) with multiphase outputs using mixed-mode-controlled delay line (MCDL). The proposed DLL uses a dual-loop technique to control various MOS capacitors and an MOS resistor in the MCDL to improve locking time and reduce static phase error. The chip was fabricated using a 0.35 μm standard CMOS process with a 3.3 V supply voltage. The measurement results showed that the proposed DLL can operate correctly with the input clock frequency varying from 145 MHz to 245 MHz. After the DLL is locked, it can generate four-phase clocks within a single clock cycle. At 180 MHz, the measured root-mean-square jitter and peak-to-peak jitter were 10 ps and 70 ps, respectively. The total power consumption of the DLL was 15 mW, and the active area of the DLL was 0.086 mm^2. The locking time was less than 30 clock cycles.

Keywords: Digital DLL, fast-locking, multiphase outputs

1 Introduction

With the rapid progression of CMOS process technology, systems have increased operating frequency and complexity, especially in a system-on-a-chip (SoC) design. Because of variations in the process, voltage, temperature, and loading (PVTL), the clock skew and phase may occur in different sub-circuits during the signal transferring process. These phenomena influence system performance considerably. Delay-locked loops (DLLs) and phase-locked loops (PLLs) are two types of clock synchronization circuits reported to solve the clock skew and jitter problems, and are used widely in high-speed microprocessors, DSPs, memory interfaces, and communications applications [1,2].

Compared with PLLs, the concept of the DLL is simpler and easy to understand. Unlike the PLL, delay line structure is employed in the DLL rather than a ring oscillator. Therefore, the jitter performance of the DLL is better than that of the PLL because no clock jitter accumulation exists. Furthermore, the DLL is a first-order system, therefore unconditionally stable and has a smaller chip area than a PLL, which contains at least two poles in the system. Consequently, the DLL is often preferred to the PLL. Generally, DLLs can be classified into two categories: analog DLLs (ADLLs) and digital DLLs (DDLLs). Compared with the ADLL, the DDLL has shorter locking time, smaller chip area, lower power consumption and standby current. Moreover, the DDLL is less process-variation sensitive and can be migrated easily to future process technologies with less redesign [3,4,5].

DDLLs can be categorized by the following control schemes: shift register-controlled DLL (SRDLL) [2], counter-controlled DLL (CDLL) [1,6,7], successive approximation register-controlled DLL (SAR-DLL) [3,4,5,8], and time-to-digital converter DLL (TDC-DLL) [9,10]. A conventional SAR-DLL has a fast locking time because of the nature of the binary search algorithm. For example, a 3-bit SAR-DLL requires only three steps to complete the locking process. However, the operation of the SAR is irreversible. Therefore, if the SAR control loop is used alone, the system becomes equally open-loop after lock-in and never tracks PVTL variations. As a result, the phase error may become relatively large and can potentially result in a system wide failure [3]. To solve these problems, a DLL uses the SAR controller as a

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coarse tuning mechanism. This study proposes an up/dn counter with binary-weighted DAC as a fine tuning mechanism. It can effectively reduce static phase error and track PVTL variations dynamically.

2 Architecture and Operating Principle of the Proposed DLL

The architecture of the proposed fast-locking DDLL with multiphase outputs using mixed-mode-controlled delay line (MCDL) is shown in fig. 1. It is composed of an initial circuit (IC), a coarse tune (CT) loop, a fine tune (FT) loop, and a MCDL. The CT loop consists of a phase comparator (PC) and a successive approximation register (SAR) controller [5,8]. The FT loop is composed of a phase detection unit (PDU), an up/dn counter, and a digital-to-analog converter (DAC) [7]. The PDU consists of a timing control unit (TCU), a phase detector (PD) [11], and a fine tune control unit (FTCU).

The DLL operation flowchart is shown in fig. 2. The initial circuit produces reset signals to initialize the SAR controller and up/dn counter to their initial state. The PC then determines if the output clock (Out_clk) is leading or lagging the reference clock (Ref_clk) and produces a signal (Comp) indicating their lead or lag condition. The Comp signal governs the operation of the SAR controller to increase or decrease the delay time introduced by the MCDL, using a larger step until the Out_clk is located within the predetermined detection window (t_c) of the PC, which is 300 ps. After the CT loop completes the locking procedure, the lock detective signal (Ld) is set to high to enable the FT loop. The PDU then generates signals Up_F and Dn_F depending on the lead or lag condition between the Out_clk and Ref_clk. The up/dn counter then counts up or down to increase or decrease the delay time introduced by the MCDL in more precise steps until the phase difference resides in the detection window (t_f) of the PDU, which is 30 ps. The proposed DLL then completes the locking procedure.

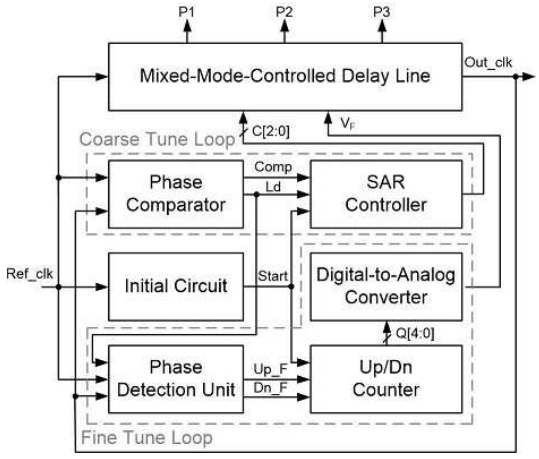

Fig. 1: The architecture of the proposed DLL

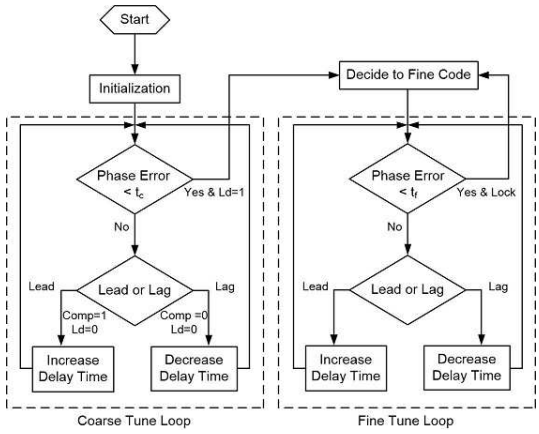

Fig. 2: The flowchart of the proposed DLL

3 Circuit Descriptions

3.1 CT Loop

The CT loop comprises a phase comparator (PC) and a SAR controller. The SAR controller is composed of a 3-bit SAR and a SAR initial circuit. The CT loop uses the PC to detect the relationship between the Out_clk and Ref_clk and the SAR for faster locking time. Each sub-circuit is introduced in the following subsections.

3.1.1 PC

The structure and timing diagram of the PC are shown in fig. 3 [5]. Two clock signals B and C are generated from the Out_clk using delay buffers with different delay times to form the detection window (t_c). The other delay buffer is used to generate clock signal A from the Ref_clk. Signal A is within the detection window if the phase difference between the Out_clk and Ref_clk is less than half the t_c. Output signals Comp and Ld are then generated under various conditions. If the Out_clk lags behind the Ref_clk, signal A is out of the lock detection window, and both the Comp and Ld signals are set to low. In contrast, if the Out_clk leads the Ref_clk, signal A is still out of the lock detection window and the Comp signal is set to high, whereas the Ld signal stays low. When the phase difference between the Out_clk and Ref_clk is less than half the t_c, signal A is located within the lock detection window and the Ld signal is set to high, denoting that the CT loop is completed and enabling operation of the FT loop.

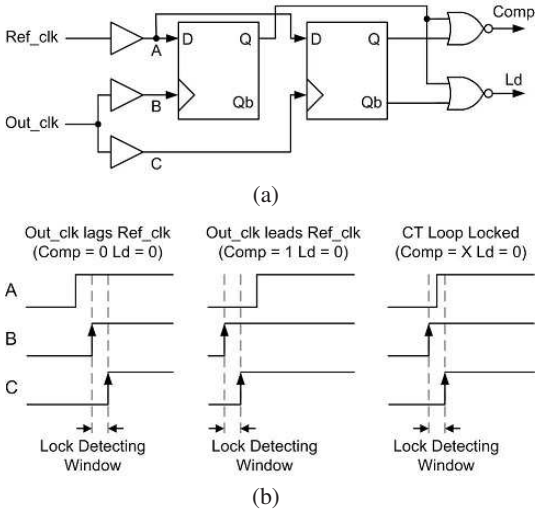

Fig. 3: (a) The structure of the PC (b) The timing diagram of the PC

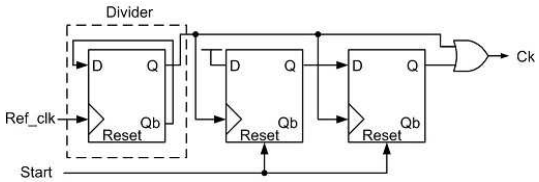

Fig. 4: The structure of the SAR initial circuit

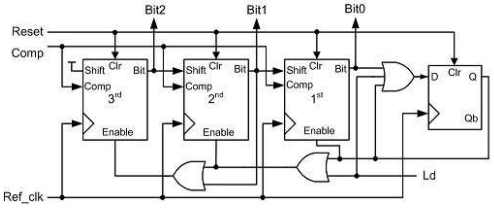

Fig. 5: The structure of the 3-bit SAR

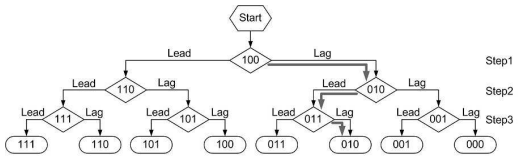

Fig. 6: The flowchart of the 3-bit SAR

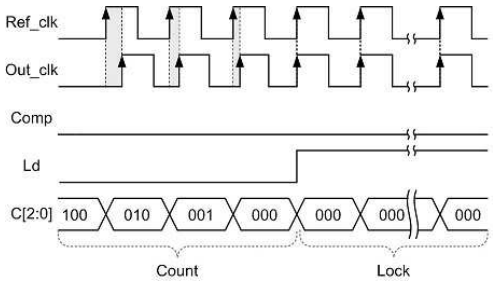

Fig. 7: The timing diagram of the CT loop when Out_clk lags behind the Ref_clk

3.1.2 SAR Controller

The SAR controller is composed of a SAR initial circuit and a 3-bit SAR. Fig. 4 shows the structure of the SAR initial circuit. It is required because outputs from the PC have a delay time before being received by the SAR. The delay time comprises the transmission delay of the Ref_clk, the feedback delay of the delay line, and the operation delay of the PC. If the frequency of Ref_clk is too high, the SAR may be unable to sustain the operation, which leads to an error output. Therefore, a SAR initial circuit is needed to reduce the sampling time of the SAR, to avoid such a condition.

Fig. 5 shows the block diagram of a 3-bit SAR [5], which is used to realize a binary search algorithm in the CT loop to decrease the maximum required locking cycle. Based on the output from the PC, the SAR determines each bit of the digital control code used in coarse tuning by using a sequential and irreversible approach.

The proposed DLL uses a 3-bit SAR, and the initial value is set to $(100)_2$. If the Comp signal is at high while the Ld signal is at low, the MSB of the SARs output remains high. Conversely, if both the Comp and Ld signals are at low, the MSB of the SARs output is set to low. This process is repeated for each subsequent bit until the least significant bit (LSB) is determined. The flowchart of the 3-bit SAR is shown in fig. 6. It requires at most three steps to complete the searching process.

However, the operation of the conventional SAR is generally irreversible. Therefore, once the searching process is completed, the system becomes open-loop and never tracks the PVTL variations. As a result, the phase error may become relatively large, which is the reason we use a FT loop with a CT loop. Finally, the CT loop timing diagram when the Out_clk lags behind the Ref_clk is shown in fig. 7 to demonstrate the operation of the CT loop.

3.2 FT Loop

The FT loop is used with the CT loop to reduce static phase error and dynamically track PVTL variation. It is composed of a phase detection unit (PDU), a 5-bit up/dn counter, and a digital-to-analog converter (DAC). Each is introduced in the following subsections.

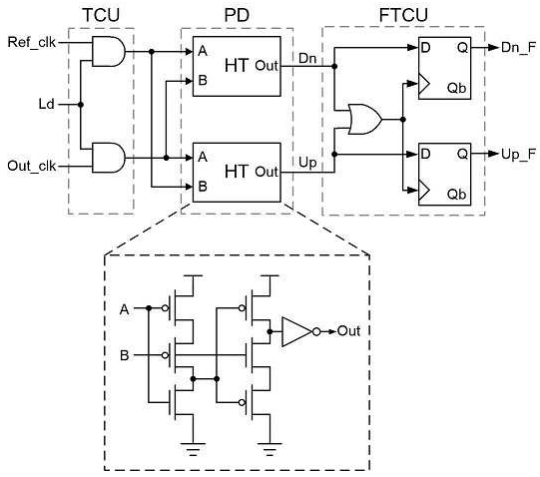

Fig. 8: The structure of the PDU

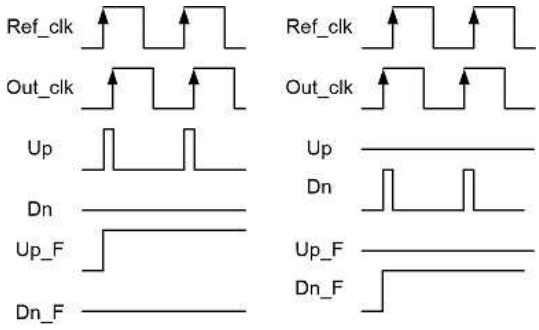

Fig. 9: The timing diagram of the PDU

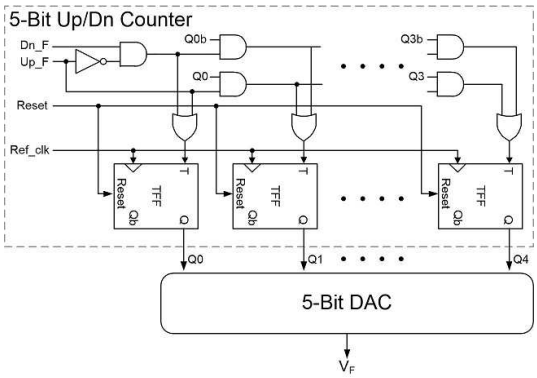

Fig. 10: The structure of the 5-bit up/dn counter and the DAC

3.2.1 PDU

Fig. 8 shows the structure of the PDU. It is composed of a timing control unit (TCU), a phase detector (PD), and a fine tune control unit (FTCU). The purpose of the TCU is to detect if the CT loop is completed. If completed, then the TCU enables the fine tune loop. A dynamic CMOS PD is used to reduce the dead zone and increase the speed of operation frequency. The PD is composed of two dynamic CMOS half transparent (HT) registers suitable for fast operation.

The PD is used to detect the relationship between the Out_clk and Ref_clk. If the Out_clk lags behind the Ref_clk, an Up pulse is generated and the FTCU converts it to a fixed DC signal, Up_F. Conversely, if the Out_clk leads the Ref_clk, a Dn pulse is generated and the FTCU converts it to a fixed DC signal, Dn_F. When the phase difference is within the dead zone of the PD, both Up and Dn pulses are generated. Up_F and Dn_F are then both be set to high by the FTCU, indicating that the lock procedure is completed. The PDU timing diagram is shown in fig. 9 to demonstrate the operation of the PDU.

3.2.2 Up/Dn Counter and DAC

The structures of the 5-bit up/dn counter and 5-bit DAC are shown in fig. 10. The output signal of the FTCU is fed into the 5-bit up/dn counter. If signal Up_F is at a high logic level and signal Dn_F is at a low logic level, the 5-bit up/dn counter starts to count up. Conversely, if signal Dn_F is at a high logic level and signal Up_F is at a low logic level, the 5-bit up/dn counter starts to count down. Using a 5-bit DAC, the output of the up/dn counter, Q[4:0], is converted to a certain DC voltage level. The voltage level is used to control the equivalent resistance of the MOS transistor, M_F, in MCDL, producing 32-step RC delay times. The initial value of the Q[4:0] is $(01000)_2$ and the maximal value is $(11111)_2$. This process is repeated until Out_clk is located within the dead zone of the PD (t_f). Under this condition, the locking procedure is completed, and Up_F and Dn_F signals are set to high, and the counter stops counting. If the Out_clk and Ref_clk are out of phase again because of PVTL variations, then the up/dn counter starts to count up or down again to track the variations. Finally, the FT loop timing diagram is shown in fig. 11 to demonstrate the operation of the FT loop.

3.3 MCDL

Fig. 12 shows the structure of the MCDL. It uses MOS switches, C[2:0], and MOS capacitors to produce different RC delay times. In the proposed DLL, the delay line is composed of four identical delay elements (DEs), resulting in uniform four-phase outputs. Each DE comprises two delay cells, a dynamic delay cell (DDC) and a fixed delay cell (FDC). Switches C[2:0] are controlled by the output of the SAR to increase or decrease the delay time in greater steps to reduce the

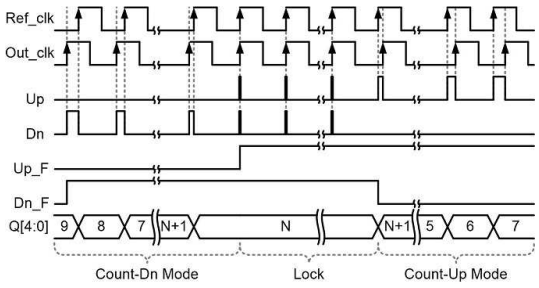

Fig. 11: The timing diagram of the FT loop

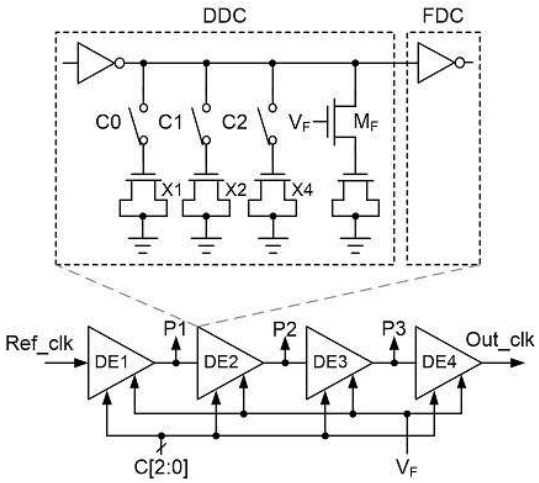

Fig. 12: The structure of the MCDL

required lock time. The fine tune transistor, M_F, acts as a MOS resistor. By controlling the gate bias, V_F, the equivalent resistance can be adjusted to provide different delay times. The gate bias, V_F, is generated using a 5-bit DAC, producing 32 output voltage steps for fine tune delay times generation. The FDC is used to provide extra delay time and to increase the driving capability for the next stage.

3.4 Initial Circuit

The initial circuit is used to initialize the system at the startup to avoid unknown conditions. The initial circuits structure and timing diagrams are shown in fig. 13(a) and fig. 13(b), respectively. The system wide reset function is also implemented in the initial circuit. When the system runs into failure, a reset pulse is generated to re-initialize the system.

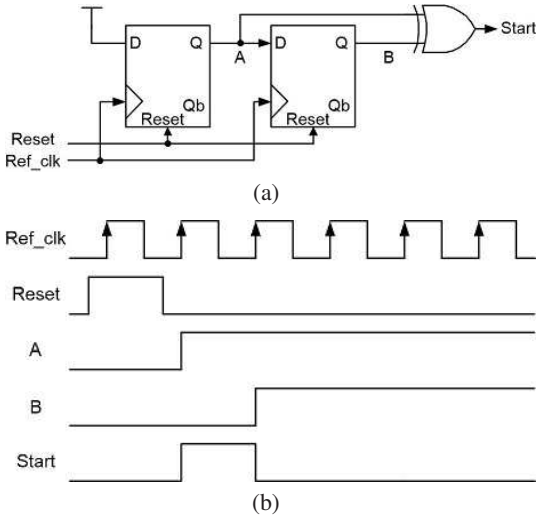

Fig. 13: (a) The structure of the initial circuit (b) The timing diagram of the initial circuit

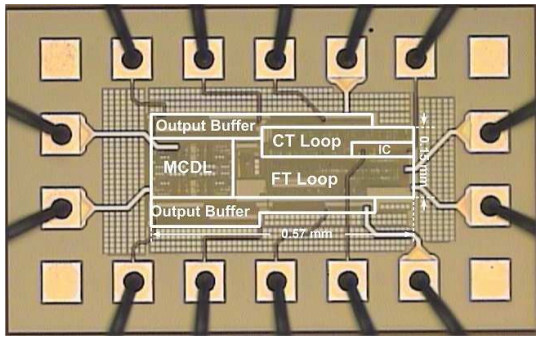

Fig. 14: The chip micrograph of the proposed DLL

4 The Simulation and Measurement Results

The chip is fabricated using a 0.35 μm standard CMOS process with a 3.3-V supply voltage. Fig. 14 shows the proposed DLLs chip micrograph; the active area is $0.15\times0.57\ mm^2$. Fig. 15 shows the delay time of the MCDL with coarse resolution versus the digital code. Fig. 16 shows the delay time of the MCDL with fine resolution versus the digital code. The simulation results of the locked waveform with a 180 MHz operating frequency are shown in fig. 17. The locking time is 19 clock cycles, including initialization, coarse tuning, and fine tuning.

The measurement results of the locked waveform with a 180 MHz operating frequency are shown in fig. 18. Fig. 19 shows the waveform of Out_clk and the second phase output (P2) of the MCDL at 180 MHz. They have a 180° phase difference. This means the Out_clk and P2 are

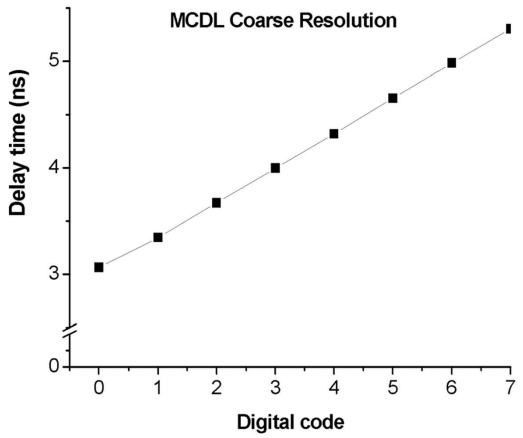

Fig. 15: The simulation results of delay time of the MCDL with coarse resolution versus the digital code

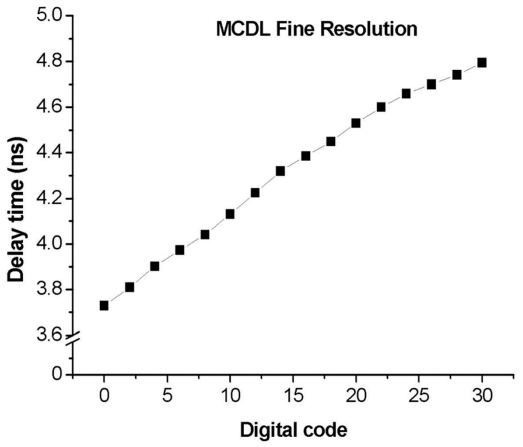

Fig. 16: The simulation results of delay time of the MCDL with fine resolution versus the digital code

in antiphase and verifies the multiphase outputs characteristic.

Fig. 20 shows the static phase error between Out_clk and Ref_clk. At 180MHz, the measured mean value of the static phase error is 31.05 ps. Fig. 21 shows the jitter histogram of the DLL clock output at 180 MHz; the measured root-mean-square (RMS) jitter is 10 ps and the peak-to-peak jitter is 70 ps (> 10,000 hits). The comparison between the proposed DLL and previous work is displayed in Table 1, which shows that the required locking time of the proposed DLL is less than references [1] and [10]. For chip area and power consumption, this study is superior to ref [10], which uses the same process technology and supply voltage as this study.

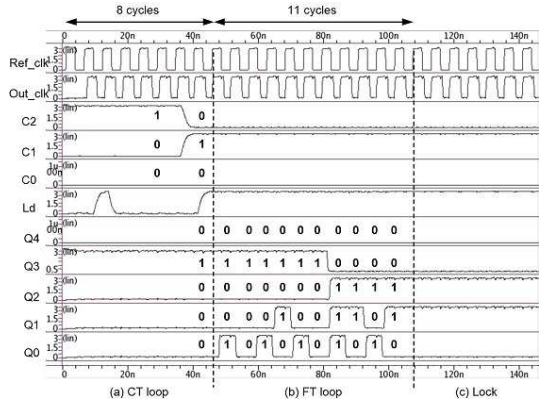

Fig. 17: The simulation locked waveform at 180 MHz

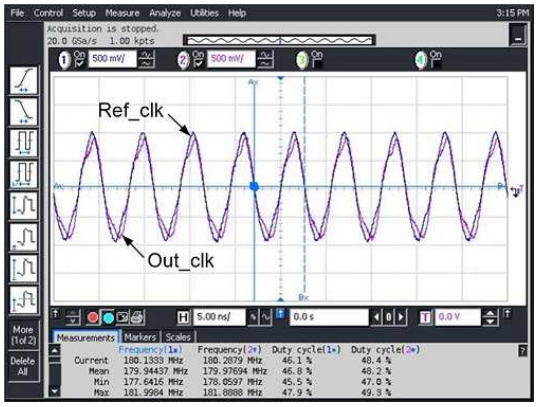

Fig. 18: The clock waveforms of output clock and reference clock at 180 MHz

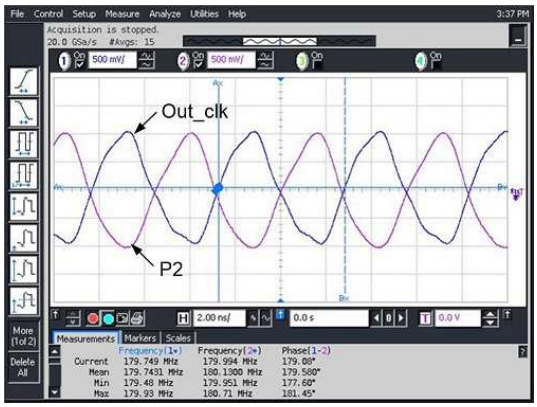

Fig. 19: The clock waveforms of output clock and phase 2 at 180 MHz

Table 1: Performance comparison

Performance Parameter	REF [1]	REF [7]	REF [10]	This work
Technology	0.18 μm	0.13 μm	0.35 μm	0.35 μm
Supply	1.8 V	1.2 V	3.3 V	3.3 V
Frequency Range	510 MHz∼1.1 GHz	15 MHz∼600 MHz	20 MHz∼85 MHz	145 MHz∼245 MHz
Jitter (peak-peak)	20.4 ps @800 MHz	8.9 ps @600 MHz	<310 ps	70 ps @180 MHz
Multiphase	4	12	7	4
Locking Time	<80 cycles	4 cycles coarse lock	<124 cycles	<30 cycles
Power Consumption	12 mW	20 mW	85.5 mW @85 MHz	15 mW @180 MHz
Active Area	0.016 mm^2	0.376 mm^2	1.9 mm^2	0.086 mm^2

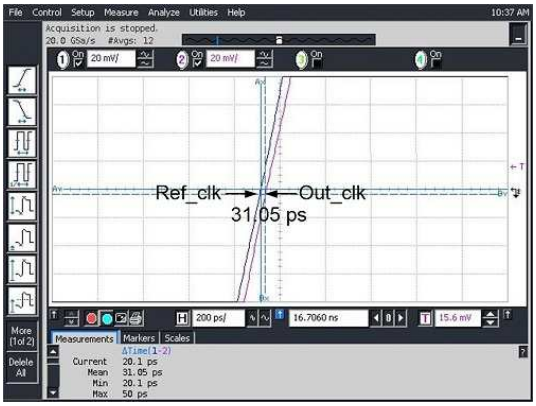

Fig. 20: The static phase error waveform at 180 MHz

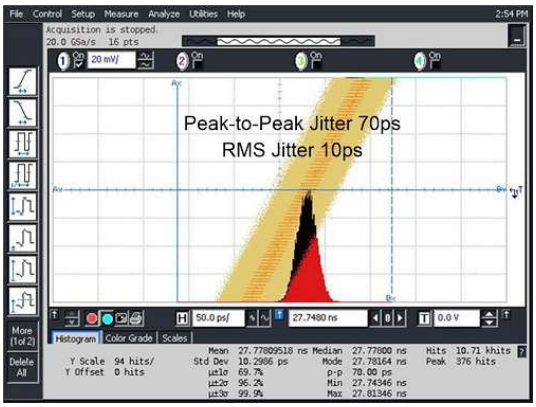

Fig. 21: The jitter histogram waveform at 180 MHz

5 Conclusions

Based on a 0.35 μm standard CMOS process, this paper proposes a fast-locking DDLL with multiphase outputs using MCDL. Using CT and FT loops achieves fast locking and minimizes static phase error. The proposed DLL can operate with input frequency varying from 145 MHz to 245 MHz. At 180 MHz, the measured static phase error is 31.05 ps, the peak-to-peak jitter is 70 ps, the RMS jitter is 10 ps, and the power consumption is 15 mW. The proposed MCDL can generate uniform four-phase outputs in a single cycle after lock-in. A new structure of DLL is introduced in this paper. If it is realized using a more advanced process technology, performance will improve. With these advantages, the proposed multiphase DLL will be suitable for a wide variety of high-speed applications, such as clock and data recovery, transmitter circuits, and frequency multipliers [12,13,14,15].

Acknowledgement

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