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An Area Efficient Approach: Comparative Analysis of Multiplier Circuits

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Abstract: Improvements in the performance of integrated circuits include scaling of transistor size and reduction of operating voltage. Smaller area and power dissipation have also taken care of for fabrication of high performance. Optimizing the power consumption, speed, area and delay of the multiplier are a major issue. In this article, the best solution to this problem is determined. As we know, Adders and Multipliers are key components of many high performance systems. By designing different multipliers, implementing their components is better to choose an option between CSL, DPL & CPL adders in fabricating different systems. This article focuses on the comparison between two algorithms for multiplication, Array and Wallace Tree. The implementation of these algorithms is performed by designing $(4\times4 and 8\times8)$ bit multiplier blocks in 0.18μ C MOS technology using EDA Tanner v.13 (evaluation version) framework tools. Furthermore, the 8-bit multipliers on GDI adder cells are compared using EDA Tanner. Multiplier design in this article provides the low power requirement and presents an area efficient approach. Moreover, number of transistors is also less as compared to CMOS for any design.

Keywords: CSL, DPL, CPL, GDI

1 Introduction

Digital multiplication is one of the most basic functions in a wide range of algorithms. Being the slowest element in the system, the performance of the system is determined by the performance of the multiplier block. Today multiplication is not only implemented with a sequence of addition, subtraction and shift operations. Many speed effective and power effective algorithms have been evolved depending upon the use in an application. From a delay perspective, algorithms place two constraints on multiplication: latency and throughput. Latency is the real delay of computing a function, a measure of how long after the inputs to a device are stable, is the final result available on the outputs. Throughput is a measure of how many multiplications can be performed in a given amount of time. Multiplier [1] in addition to a high delay block is also a major source of power dissipation, many algorithm are designed with the help of digital multiplication. So it is of great interest to identify and apply algorithms which has less delay as well as less power consumption of the multiplier i.e. which has smaller power delay product and fast processing.

Bulks of both NMOS and PMOS are connected to N or P (respectively), so it can be arbitrarily biased at contrast with a CMOS inverter.

2 Preliminaries

A. Logic Equations for the Proposed Full Adders

The equations presented below can be stated as follows:

$$Sum = A \oplus B \oplus Cin \tag{1}$$

$$Sum = \overline{A} \oplus \overline{B} \oplus \overline{C}in \tag{2}$$

$$Sum = C\overline{in}(A \oplus B) + Cin(A\overline{\oplus}B) \tag{3}$$

$$Cout = A.(A \oplus \overline{B} + C\overline{in}(A \oplus B)) \tag{4}$$

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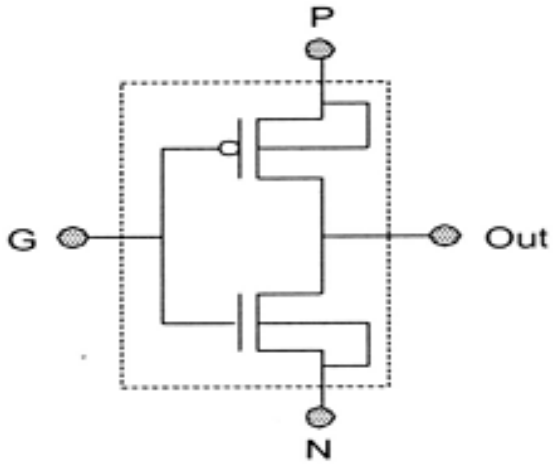

Fig. 1: GDI basic cell [2]

Table 1: Various logic functions of GDI cell for different cell for different input configurations

N	P	G	Out	Function
'0'	B	A	$\bar{A}B$	F1
B	'1'	A	$\bar{A}+B$	F2
'1'	B	A	$A+B$	OR
B	'0'	A	AB	AND
C	B	A	$\bar{A}B+AC$	MUX
'0'	'1'	A	$\bar{A}$	NOT

B. XOR and XNOR gates based on GDI cell

The XOR and XNOR gates based on GDI cells are applications of the GDI technique. As can be seen in Fig. 2, each of them requires only four transistors. Obviously, the proposed GDI XOR and XNOR gates use less transistors compared with the conventional CMOS counterparts [3].

C. Full Adders Based on GDI XOR and XNOR Gates

According to the logic equations mentioned above and the GDI XOR and XNOR gates in Fig. 2,

Full adders can be, GDI based XOR full adder and GDI based XNOR full adder. Each of the two full adders includes 10 transistors. Figure 3 shows gate level design of full adder. Due to the advantages of GDI cell, this circuit still can achieve its benefit of low power consumption. This scheme also includes three modules.

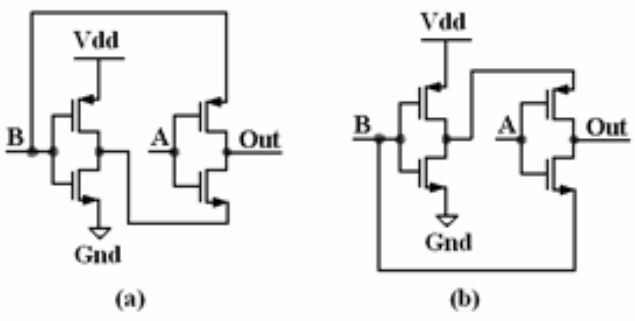

Fig. 2: (a) GDI based XOR gate (b) GDI based XNOR gate [4]

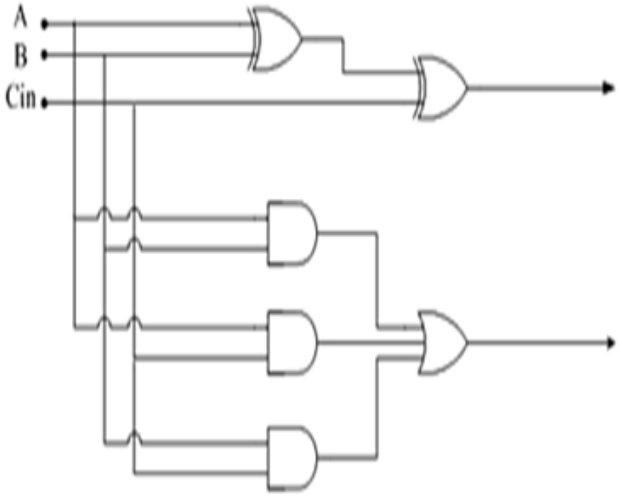

Fig. 3: Gate level based of full adder [1]

Figure 4 and 5 shows GDI based XOR and XNOR Full adders [5].

3 Multiplication Algorithms

There are numerous multiplier [6] implementations, some of them are good in terms of power dissipation [7] and some have better performance in terms of delay [8]. In this section 8-bit array and tree multiplier algorithms are discussed.

A. Array Multiplier

An $n \times n$ array of AND gates can compute all the $a_i b_i$ terms simultaneously. The terms are summed by an array of $'n[n-2]'$ full adders and 'n' half adders. The delay of this block is a function of the number of rows [9], O (n), which is a big improvement over the simple-minded scheme of using conventional adders for each row. Figure 6 shows 4×4 array multiplier and Figure 7 shows 4×4 Tree Multiplier. Figure 8 and 10 shows actual layouts of GDI based XOR and XNOR Full adders circuits whereas

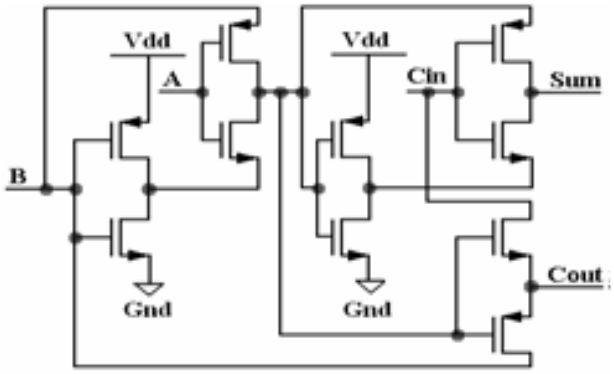

Fig. 4: GDI Based XOR full adders

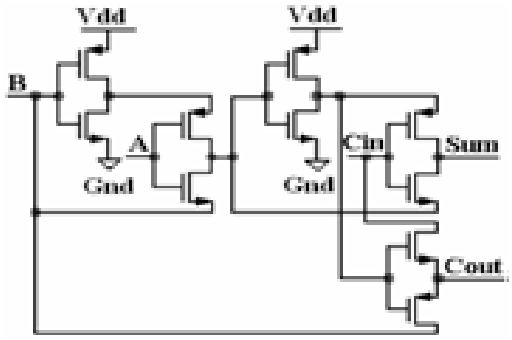

Fig. 5: GDI based XNOR full adder [3]

Table 2: Comparative analysis of 8-bit multipliers

PARAMETERS	CPL ARRAY	CPL TREE	CSL ARRAY	CSL TREE	DPL ARRAY	DPL TREE
Number of Transistors	1472	1472	1952	1952	2336	2336
Power Consumption	3.77 X 10^{-4}	6.24 X 10^{-4}	6.36 X 10^{-4}	1.82 X 10^{-4}	3.50 X 10^{-4}	3.24 X 10^{-4}
Delay	1.01 X 10^{-10}	4.11 X 10^{-11}	5.32 X 10^{-11}	6.75 X 10^{-11}	1.11 X 10^{-10}	6.12 X 10^{-11}

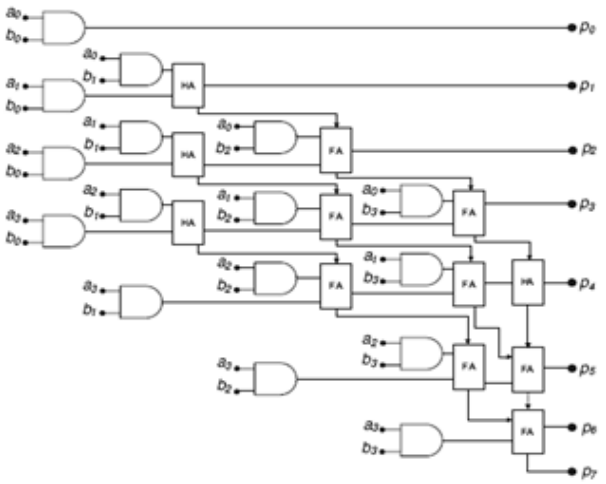

Fig. 6: Block diagram of 4×4 array multiplier [11]

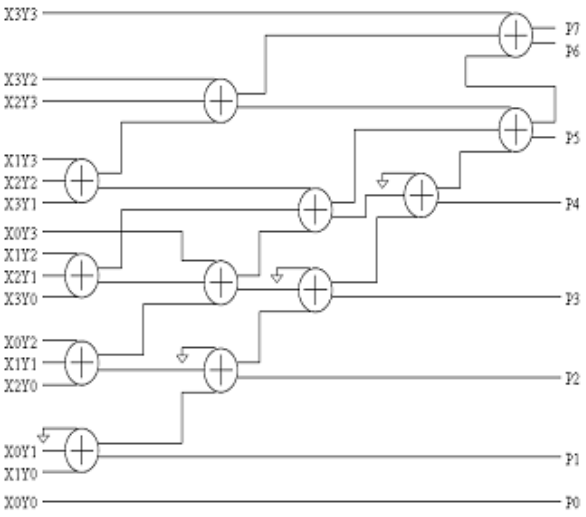

Fig. 7: 4×4 Tree Multiplier

Figure 9 shows an AND gate. Optimizing [10] the power consumption, speed, area and delay of the multiplier are major issues, whose best solution is considered in this section.

1) Tree Multiplier

The advantage of Wallace tree is speed because the addition of partial products is O (log N) where N is the number of summands

4 Simulation and Comparison

A. Simulation Environment: Array and tree multipliers based on GDI XOR and GDI XNOR adder cells are simulated in EDA Tanner (Evaluation version). All the results are obtained in 180nm CMOS process technology.

Comparison: 8-bit array and tree multipliers are compared based on the parameters, delay and number of transistors. Comparative analysis of 8-bit multipliers using GDI based adder cells working at 400MHz is done with 8-bit CMOS multiplier as shown in the table 2.

5 Conclusions

Multiplier design in this paper work provides the low power requirement. It also presents an area efficient approach to low power, less number of transistors as

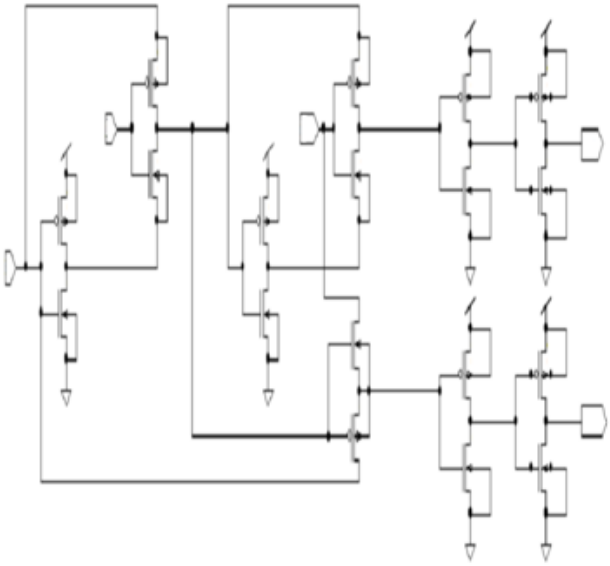

Fig. 8: GDI Based XOR full adder

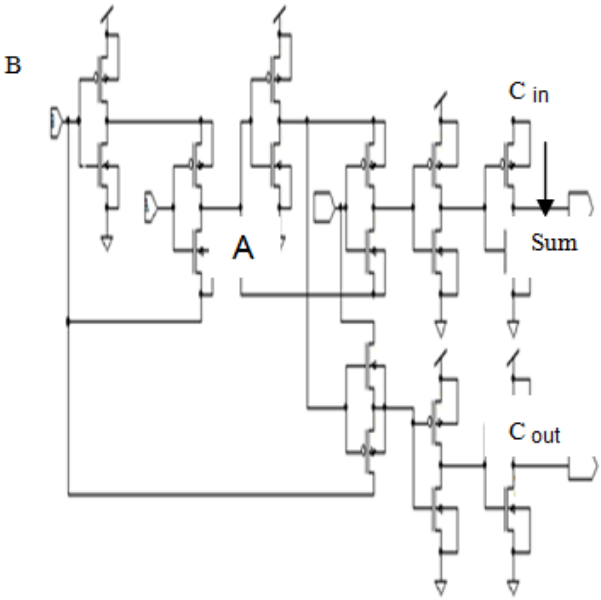

Fig. 10: GDI Based XNOR full adders

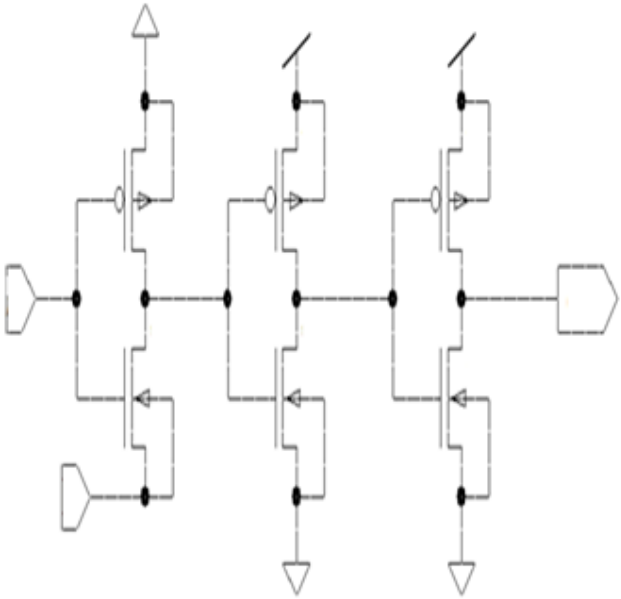

Fig. 9: Schematic of AND Gate

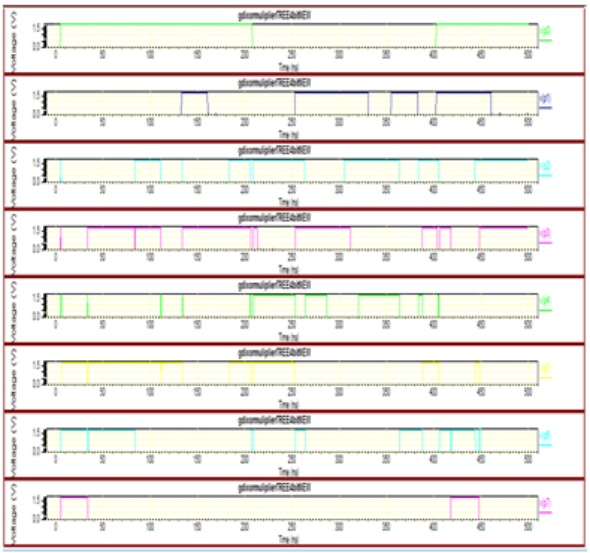

Fig. 11: Output waveform of 8-Bit Tree Multiplier Using GDI XOR Based Adder Cells

compared to CMOS and DCVS for any design. 8-bit multipliers were designed in Tanner (Evaluation version) tool using 180nm and analysis of dynamic power dissipation, delay and area was done. The results in table 2 are at frequency 400MHz and load capacitance is 1pF. Channel length for both NMOS & PMOS is 180nm and width is 1790nm for PMOS & 699nm for NMOS transistor.

6 Future scope

As a future scope of the work, Power of the circuit can be further reduced if requirement of buffers in the circuit is avoided. Also, this technique can be compounded with other methods used such as using sleep transistors, dual threshold CMOS, dynamic threshold CMOS. This article work is based on combinational circuit design. Techniques can also be applied to sequential circuits. The

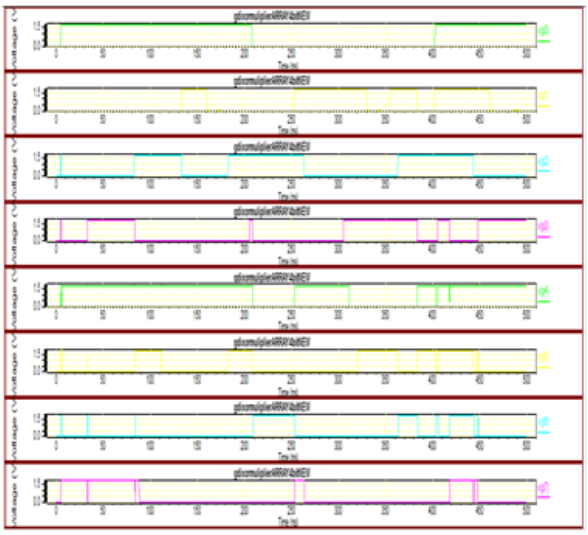

Fig. 12: Output Waveform of 8-Bit Array Multiplier Using GDI XOR Based Adder Cells

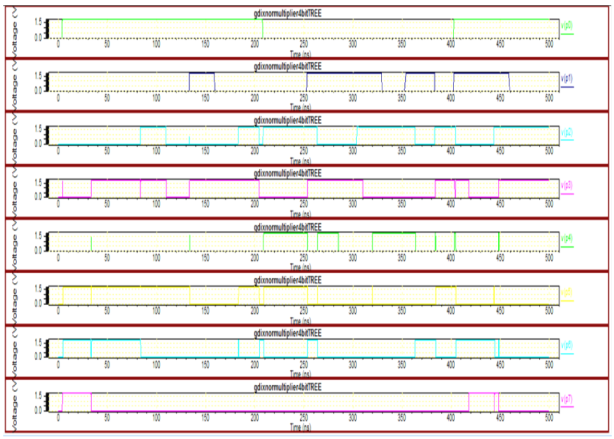

Fig. 13: Output waveform of 8-Bit Tree Multiplier Using GDI XNOR Based Adder Cells

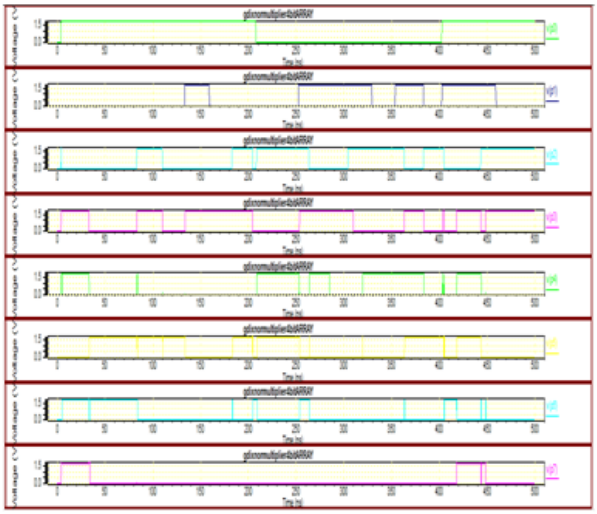

Fig. 14: Output waveform of 8-Bit Array Multiplier Using GDI XNOR Based Adder Cells

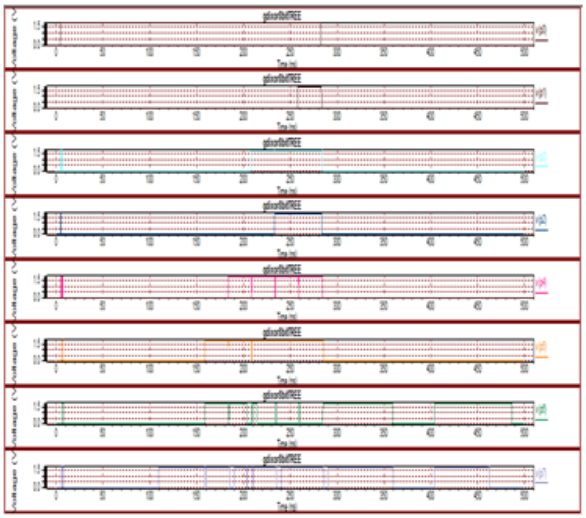

Fig. 15: Output waveforms from p0 to p7 of 8-Bit Tree Multiplier Using GDI XOR Based Adder Cells

work can be extended for the calculation of SPC as this article work mainly concentrates on the DPC of the total power consumption. In VLSI design CSL technique has very good scope for future because of less power consumption.

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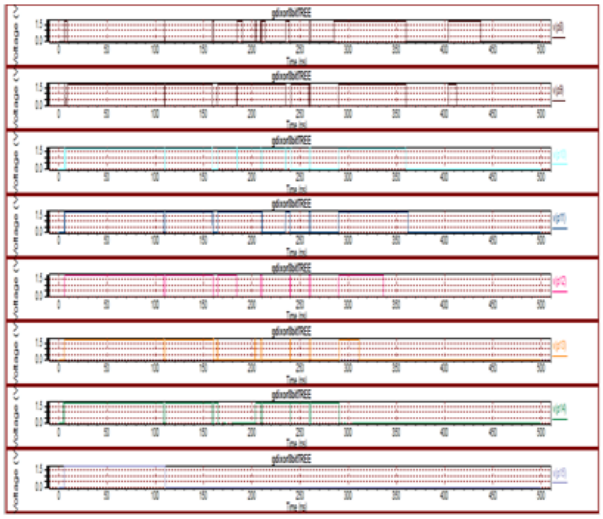

Fig. 16: Output waveforms from p8 to p15 of 8-Bit Tree Multiplier Using GDI XOR Based Adder Cells

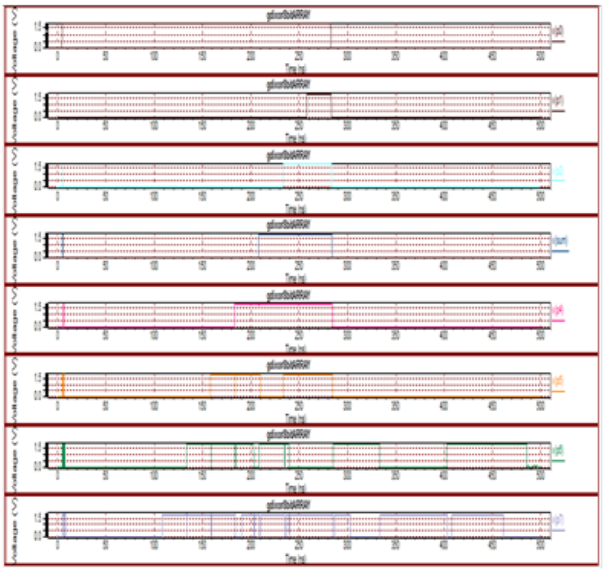

Fig. 17: Output waveforms from p0 to p7 of 8-Bit Array Multiplier Using GDI XOR Based Adder Cells

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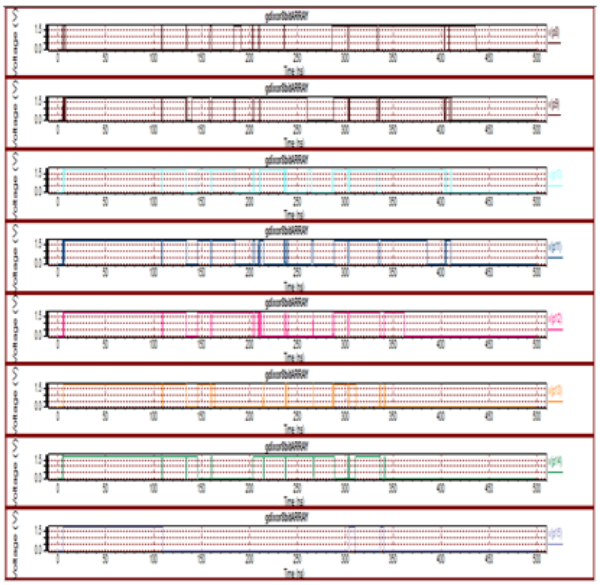

Fig. 18: Output waveforms from p7 to p15 of 8-Bit Array Multiplier Using GDI XOR Based Adder Cells

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