Advanced Engineering Technology and Application
An International Journal

http://dx.doi.org/10.12785/aeta/paper

D Flip Flop with Different Technologies

Amit Grover[1,*] *and Sumer Singh*[2]

[1] Department of Electronics & Communication Engineering, S.B.S State Technical Campus Ferozepur, Punjab, India
[2] Department of Electronics & Communication Engineering, Government Polytechnic College, Ferozepur, Punjab, India

Received: 15 Oct. 2013, Revised: 19 Dec. 2013, Accepted: 22 Dec. 2013
Published online: 1 Jan. 2014

Abstract: This article explains a new implementation of efficient D-Flip-Flop (DFF) using Gate-Diffusion-Input (GDI) technique, PowerPC, DSTC, and HLFF. This DFF design allows reducing power-delay product and area of the circuit, while maintaining low complexity of logic design. Performance comparison with other DFF design techniques is presented, with respect to gate area, number of devices, delay and power dissipation, showing advantages and drawbacks of GDI DFF as compared to other methods. The performance is carried out by HSPICE simulation with 180 nm & 90 nm CMOS technology.

Keywords: D flip-flop, low power, Gate-Diffusion-Input (GDI) technique, PowerPC, DSTC, and HLFF

1 Introduction

Binary logic has been widely used in the electronic fields. It is traditional and thus, more mature than multiple-valued logic. However, alongside the booming of the information and electronic industry, the deficiencies of binary circuits began to emerge. It has been rather difficult for binary logic to satisfy demands from chip area, switching speed, power dissipation, and other aspects all at the same time. Therefore, multiple valued circuits are becoming increasingly important. Digital circuits in every high speed technology are typically benchmarked by the performance of static frequency dividers which is recognized as a figure of merit for a digital integrated circuit process, because a static frequency divider uses the same basic flip-flop elements found in more complex sequential circuits[1]. High speed frequency dividers [2] are one of the key devices in measurement equipments, microwave and satellite communication systems. Therefore, many different high speed static and dynamic frequency dividers [3] [4] based on various kinds of device technology have been developed.

The fastest frequency dividers [5] to date are the AlInAs/GaInAs HBT static frequency divider operating at 39.5GHz [6], the AlGaAs/GaAs HEMT and the T-gate A1GaAs/InGaAs MODFET dynamic frequency dividers at 34GHz [7] and 51GHz [8], respectively. In addition, a 30GHz static frequency divider based on the Si-bipolar technology has been reported in [9]. On the Other hand, building low power VLSI systems has emerged as highly in demand because of the fast growing technologies in mobile communication and computation. The battery technology does not advance at the same rate as the microelectronics technology [10]. There is a limited amount of power available for the mobile systems. So designers are faced with more constraints: high speed, high throughput, small silicon area, and at the same time, low power consumption. Therefore building low power, high performance circuits are of great interest [11].

Wide utilization of memory storage systems and sequential logic in modern electronics triggers a demand for high-performance and low-area implementations of basic memory components. One of the most important state-holding elements is the D-Flip-Flop (DFF) [1]. Various DFF circuits were researched and presented in the literature, aiming to achieve an optimal design in terms of delay, power and area. Some efficient techniques were developed and adopted by designers for a variety of technologies [1].

2 BASIC GDI FUNCTION

The GDI method is based on the use of a simple cell as shown in Fig. 1. At first glance, the basic cell reminds one of the standard CMOS inverter, but there are some important differences.

* Corresponding author e-mail: amitgrover_321@rediffmail.com

© 2014 NSP
Natural Sciences Publishing Cor.

1) The GDI cell contains three inputs: (common gate input of nMOS and pMOS), P (input to the source/drain of pMOS), and N (input to the source/drain of nMOS). 2) Bulks of both nMOS and pMOS are connected to N or P (respectively), so it can be arbitrarily biased at contrast with a CMOS inverter.

Gate-Diffusion-Input (GDI) design technique that was recently developed and presented in [12], proposes an efficient alternative for logic design in standard CMOS and SOI technologies. The GDI method is based on the simple cell shown in Fig. 1. A basic GDI cell contains four terminals - G (the common gate input of the nMOS and pMOS transistors), P (the outer diffusion node of the pMOS transistor), N (the outer diffusion node of the nMOS transistor) and the D node (the common diffusion of both transistors). P, N and D may be used as either input or output ports, depending on the circuit structure. Table 1 shows how various configuration changes of the inputs P, N and G in the basic GDI cell correspond to different Boolean functions at the output D. GDI enables simpler gates, lower transistor count, and lower power dissipation in many implementations, as compared with standard CMOS and PTL design techniques [12]. Multiple-input gates can be implemented by combining several GDI cells. The buffering constraints, due to possible VTH drop, are described in detail in [12], as well as technological compatibility with CMOS and SOI.

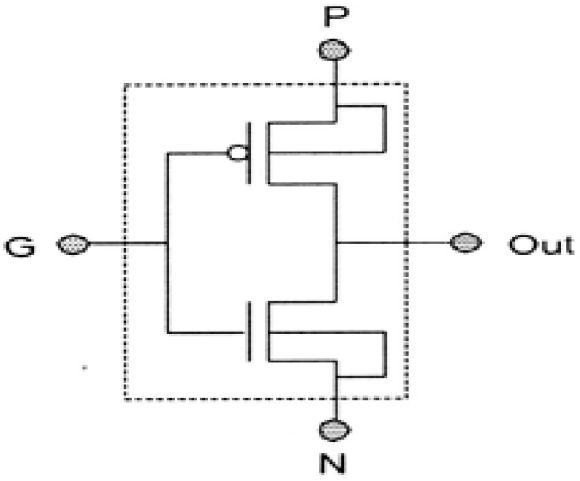

Fig. 1: GDI basic cell

It must be remarked that not all of the functions are possible in standard p-well CMOS process but can be successfully implemented in twin-well CMOS or silicon on insulator (SOI) technologies.

Table 1: VARIOUS LOGIC FUNCTIONS OF GDI CELL FOR DIFFERENT INPUT CONFIGURATIONS

N	P	G	Out	Function
'0'	B	A	$\bar{A}B$	F1
B	'1'	A	$\bar{A}+B$	F2
'1'	B	A	$A+B$	OR
B	'0'	A	AB	AND
C	B	A	$\bar{A}B+AC$	MUX
'0'	'1'	A	$\bar{A}$	NOT

3 Power Consumption in CMOS Circuits

There are three main components of power consumption in digital CMOS VLSI circuits.

1. Switching Power: consumed in charging and discharging of the circuit capacitances during transistor switching.
2. Short-Circuit Power: consumed due to short-circuit current flowing from power supply to ground during transistor switching. This power more dominates in Deep Sub Micron (DSM) technology.
3. Static Power: consumed due to static and leakage currents flowing while the circuit is in a stable state. The first two components are referred to as dynamic power, since power is consumed dynamically while the circuit is changing states. Dynamic power accounts for the majority of the total power consumption in digital CMOS VLSI circuits at micron technology [7][13].

$$P_{avg} = P_{switching} + P_{short-circuit} + P_{leakage} \quad (1)$$

$$P_{avg} = \alpha_{0\to1} \times C_l \times V_{dd}^2 \times F_{clk} + I_{sc} \times Vdd + I_{leakage} \times Vdd \quad (2)$$

4 SIMULATION AND COMPARISON

Due to the topological differences among the existing latches, some of them required a modified test bench, i.e., a dual input and/or a single output. However, these modifications did not alter the principal of the analysis approach based on the simulation conditions. The role of

© 2014 NSP
Natural Sciences Publishing Cor.

the test bench is to provide the realistic data and clock signals, the fan out signal degradation from the previous and to the succeeding stage, and measurement of power dissipated on switching of the clock and data inputs. Buffering inverters provide the realistic data and clock signals, which themselves are fed from ideal voltage sources. Furthermore, capacitive load at the data input simulates the fan out signal degradation from previous stages. Capacitive loads at the outputs simulate the fan out signal degradation caused by the succeeding stages.

As mentioned in the section on power considerations, there are three kinds of power dissipation that were measured in order to get the real insight in the amount of power consumed in and around the latch due to its presence.

1. Local data power dissipation presents the portion of the gray inverter's power consumption dissipated on switching the data input capacitance.
2. Local clock power dissipation presents the portion of the black inverter's power consumption dissipated on switching the clock input capacitance.
3. Internal power dissipation includes the intrinsic power dissipated on switching the internal nodes of the circuit and excludes the power dissipated on switching the output load capacitances.

Figure 2 and 3 shows Schematic of GDI D flip flop and its waveform.

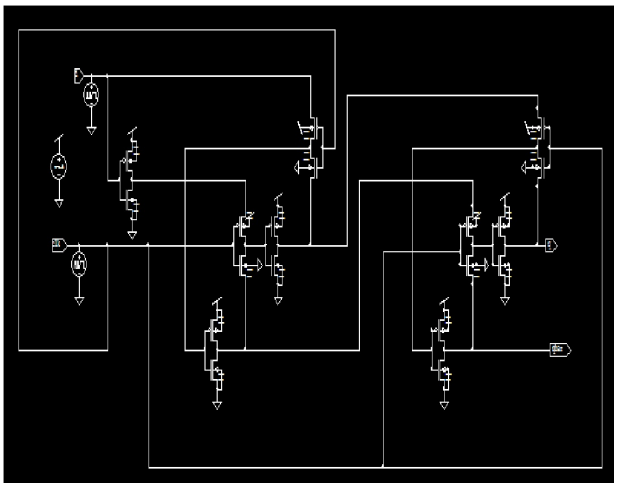

Fig. 2: GDI D Flip-flop

Figure 4 and 5 shows Schematic of DSTC and its waveform.

Figure 6 and 7 shows Schematic of POWERPC and its waveform.

Figure 8 and 9 shows Schematic of HLFF and its waveform.

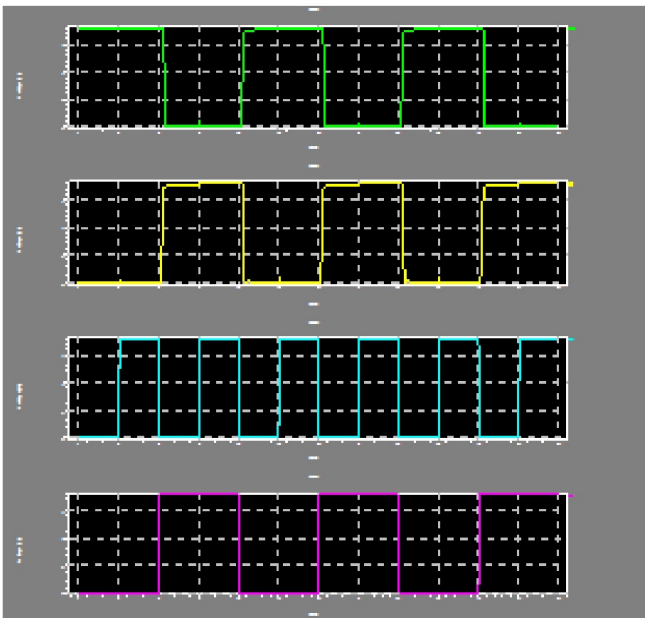

Fig. 3: Waveform of GDI D Flip-flop

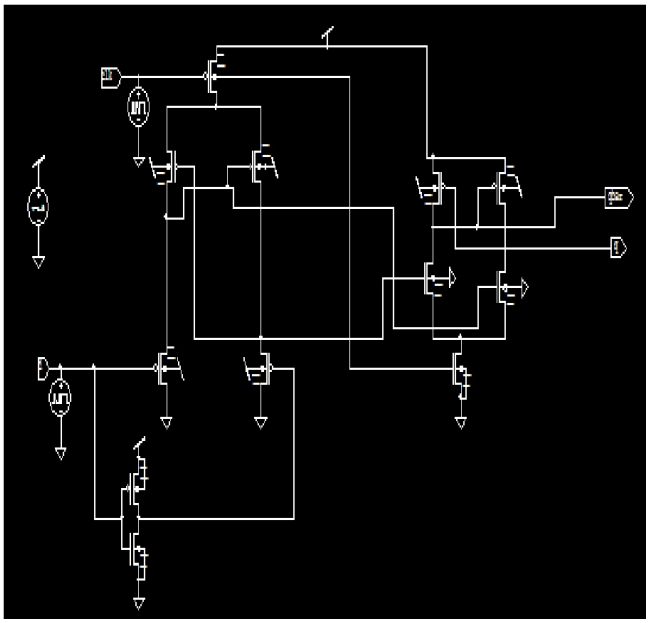

Fig. 4: Schematic of DSTC

5 FINAL RESULTS

The Final result has been carried using 180 nm and 90 nm technology with width of NMOS as .64 and of PMOS as 1.70 along with their respective lengths as 180 nm and 90nm. Table 2 shows that DSTC circuit produces lesser power dissipation as compare to D flip flop using GDI when we use 90 nm technologies as compare to 180 nm

© 2014 NSP
Natural Sciences Publishing Cor.

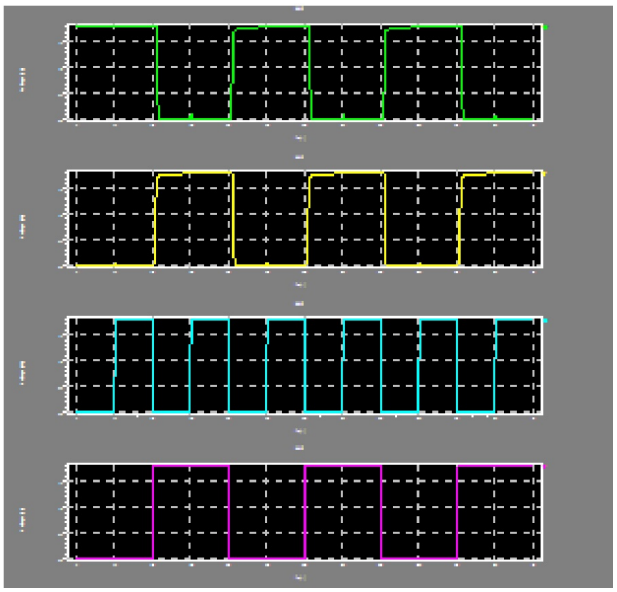

Fig. 5: Waveform of DSTC

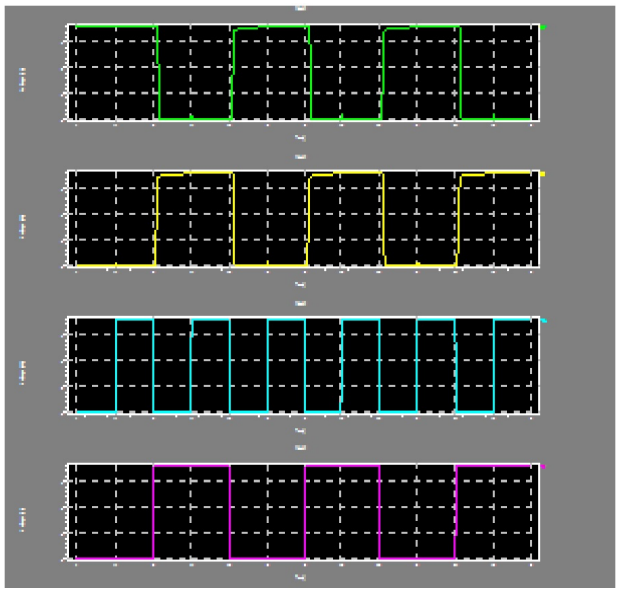

Fig. 7: Waveform of POWERPC

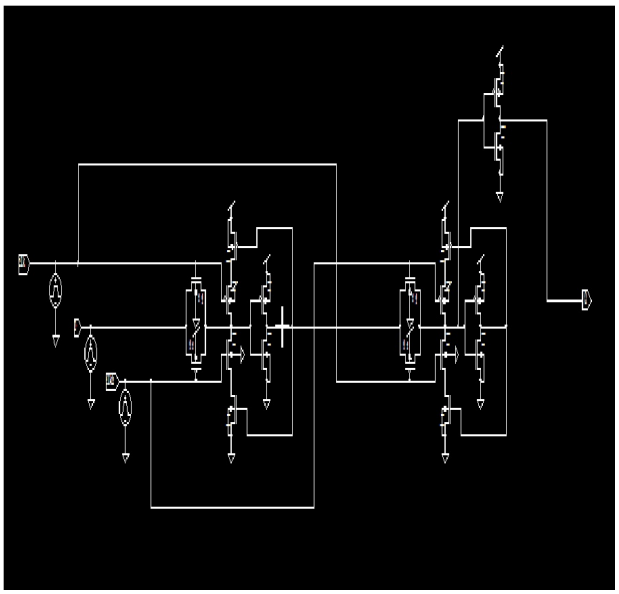

Fig. 6: Schematic of POWERPC

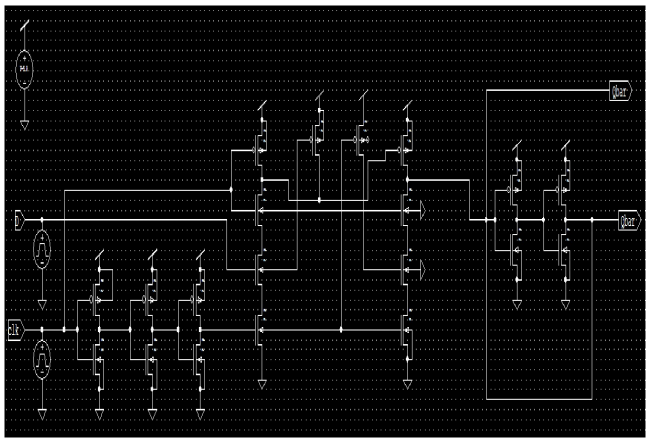

Fig. 8: Schematic of HLFF

technology. In DSTC circuit, we have used 12 transistors but in GDI number of transistors used are 18 to build D flip flop, so in DSTC lesser be the area, lesser power dissipation and lesser delay as compare to the GDI based D Flip flop. PowerPC circuit is implemented with 18 transistors so its power dissipation is more similar to the circuit GDI. HLFF circuit is implemented with 20 transistors so it dissipates more power as compare to all circuits and more is its area. This article explains the performance comparison of four different circuits which include Gate-Diffusion-Input (GDI) technique, PowerPC, DSTC, and HLFF used to build D flip-flop. Among all these circuits DSTC uses lesser transistors, lesser area, lesser delay and lesser the power dissipation. The main point of the optimization is the minimization of the power-delay product, given the always-present tradeoff between power and speed.

6 CONCLUSIONS AND FUTURE RESEARCH

A new implementation of high-performance D-Flip- Flop using Gate-Diffusion-Input technique, PowerPC, DSTC,

© 2014 NSP
Natural Sciences Publishing Cor.

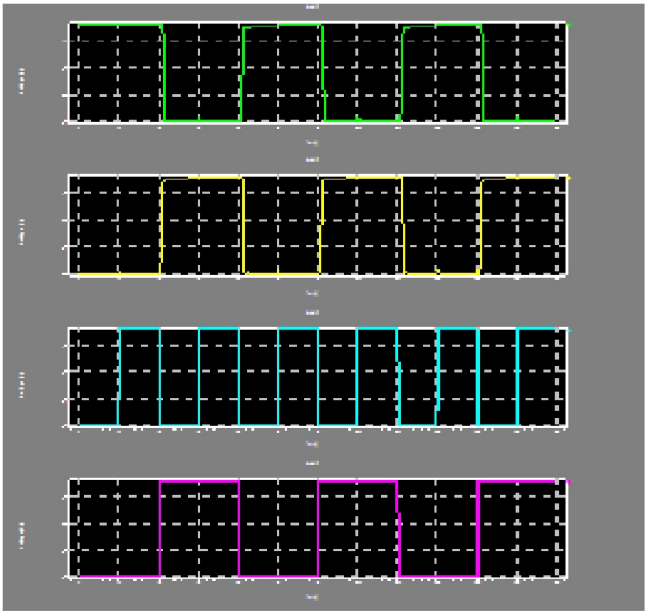

Fig. 9: Waveform of HLFF

Table 2: PERFORMANCE PARAMETERS OF D FLIP FLOP

Design Style	No. of transistors	Minimum Length (µm)	Width of NMOS (µm)	Length of PMOS (µm)	Avg. Power Consm. (watts)	Prop. Delay (nsec)	Prop. Delay Product (w/sec)
D Flip Flop using GDI Using 180 nm	18	0.18	0.64	1.7	2.27×10^{-5}	2.79	6.33×10^{-14}
D Flip Flop using GDI Using 90 nm	18	0.09	0.64	1.7	1.69×10^{-5}	1.89	3.19×10^{-14}
DSTC Using 180 nm	12	0.18	0.64	1.7	1.84×10^{-6}	2.29	4.21×10^{-15}
DSTC Using 90 nm	12	0.09	0.64	1.7	1.34×10^{-5}	1.74	2.23×10^{-15}
PowerPC Using 180 nm	18	0.18	0.64	1.7	3.17×10^{-5}	2.45	7.76×10^{-14}
PowerPC Using 90 nm	18	0.09	0.64	1.7	1.19×10^{-5}	1.65	1.96×10^{-14}
HLFF Using 180 nm	20	0.18	0.64	1.7	2.64×10^{-5}	2.81	7.41×10^{-14}
HLFF Using 90 nm	20	0.09	0.64	1.7	1.04×10^{-5}	2.34	2.43×10^{-14}

and HLFF was presented. The proposed circuit has a simple structure, based on Master-Slave principle, and contains 18 transistors. An optimization procedure was developed for GDI DFF, based on iterative transistor sizing, while targeting a minimal power-delay product. Performance comparison with other DFF design techniques was shown, with respect to gate area, number of devices, delay and power dissipation. A variety of circuits have been implemented in 90 nm and 180 nm technologies to compare the proposed GDI structure with a set of representative flip-flops, commonly used for high performance design. The future research activities may include further higher bits of D- Flip using this GDI technology, PowerPC, DSTC, and HLFF.[1]

References

[1] J. M. Rabaey, A. P. Chandrakasan, and B. Nikolic, *Digital integrated circuits*. Prentice hall Englewood Cliffs, 2002, vol. 2.

[2] M. Sokolich, C. Fields, B. Shi, Y. Brown, M. Montes, R. Martinez, A. Kramer, S. Thomas III, and M. Madhav, "A low power 72.8 ghz static frequency divider implemented in alinas/ingaas hbt ic technology," in *GaAs IC Symposium, 2000. 22nd Annual*. IEEE, 2000, pp. 81–84.

[3] M. Hafizi, J. F. Jensen, R. A. Metzger, W. E. Stanchina, D. B. Rensch, and Y. K. Allen, "39.5-ghz static frequency divider implemented in alinas/gainas hbt technology," *Electron Device Letters, IEEE*, vol. 13, no. 12, pp. 612–614, 1992.

[4] J. M. Wong, V. S. Cheung, and H. C. Luong, "A 1-v 2.5-mw 5.2-ghz frequency divider in a 0.35-μm cmos process," *Solid-State Circuits, IEEE Journal of*, vol. 38, no. 10, pp. 1643–1648, 2003.

[5] H. Wang, "A 1.8 v 3 mw 16.8 ghz frequency divider in 0.25/spl mu/m cmos," in *Solid-State Circuits Conference, 2000. Digest of Technical Papers. ISSCC. 2000 IEEE International*. IEEE, 2000, pp. 196–197.

[6] V. Stojanovic and V. G. Oklobdzija, "Comparative analysis of master-slave latches and flip-flops for high-performance and low-power systems," *Solid-State Circuits, IEEE Journal of*, vol. 34, no. 4, pp. 536–548, 1999.

[7] G. Gerosa, S. Gary, C. Dietz, D. Pham, K. Hoover, J. Alvarez, H. Sanchez, P. Ippolito, T. Ngo, S. Litch *et al.*, "A 2.2 w, 80 mhz superscalar risc microprocessor," *Solid-State Circuits, IEEE Journal of*, vol. 29, no. 12, pp. 1440–1454, 1994.

[8] H. Partovi, R. Burd, U. Salim, F. Weber, L. DiGregorio, and D. Draper, "Fa 8.5: Flow-through latch and edge-triggered flip-flop hybrid elements," *ISSCC Dig. Tech. Papers*, vol. 8, pp. 138–139, 1996.

[9] J. Yuan and C. Svensson, "New single-clock cmos latches and flipflops with improved speed and power savings," *Solid-State Circuits, IEEE Journal of*, vol. 32, no. 1, pp. 62–69, 1997.

[10] A. Morgenshtein, A. Fish, and I. A. Wagner, "Gate-diffusion input (gdi)-a novel power efficient method for digital circuits: a design methodology," in *ASIC/SOC Conference, 2001. Proceedings. 14th Annual IEEE International*. IEEE, 2001, pp. 39–43.

[11] A. Saberkari, S. B. Shokouhi, A. Kiani, and F. Poorahangaryan, "A novel low power static frequency divider based on the gdi technique," in *Electrical and Computer Engineering, 2009. CCECE'09. Canadian Conference on*. IEEE, 2009, pp. 67–70.

[12] A. Morgenshtein, A. Fish, and I. A. Wagner, "Gate-diffusion input (gdi): a power-efficient method for digital combinatorial circuits," *Very Large Scale Integration (VLSI)*

© 2014 NSP
Natural Sciences Publishing Cor.

Systems, IEEE Transactions on, vol. 10, no. 5, pp. 566–581, 2002.

[13] T. Fuse, M. Tokumasu, S. Kawanaka, H. Fujii, A. Kameyama, M. Yoshimi, and S. Watanabe, "A 1.1 v soi cmos frequency divider using body-inputting scl circuit technology," in *SOI Conference, 2000 IEEE International*. IEEE, 2000, pp. 106–107.

Amit Grover became a Member (M) of Association ISTE in 2006, a Senior Member (SM) of society SELCOME in September 2009, and a Project-In charge (PI) in august 2011 and in September 2012. The author place of birth is Ferozepur, Punjab, India on 27th, September 1980.The author received his M. Tech degree in Electronics and Communication Engineering from Punjab Technical University, Kapurthla, Punjab, India in 2008 and received his B. Tech degree in Electronics and Communication Engineering from Punjab Technical University, Kapurthala, Punjab, India in 2001. Currently, he is working as an Assistant Professor in Shaheed Bhagat Singh State Technical Campus, Ferozepur, Punjab, India. The author is a Reviewer of many Reputed International Journals. His area of interest includes signal processing, MIMO systems, Wireless mobile communication; high speed digital communications, 4G Wireless Communications and VLSI Design.

Sumer Singh the author place of birth is Ferozepur, Punjab, India on 15th, August 1985. The author received his M. Tech degree in Electronics and Communication Engineering from Punjab Technical University, Kapurthla, Punjab, India in 2013 and received his B. Tech degree in Electronics and Communication Engineering from Punjab Technical University, Kapurthala, Punjab, India in 2010. Currently, he is working as a Lecturer in Department of Electronics & Communication Engineering, Government Polytechnic College, Ferozepur, Punjab India. His area of interest includes Wireless Communication Network, Mobile Ad Hoc Network, Wireless Sensor Network and VLSI Design.

© 2014 NSP
Natural Sciences Publishing Cor.