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A New Synchronization Algorithm for Grid-Connected Inverters

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Abstract: Synchronization algorithms are of great importance in control of grid-connected inverters as an integral part of distributed power generation units such as photovoltaic systems. A new all-digital closed-loop phase-locked algorithm for the synchronization signals of three-phase grid-connected inverters is presented even considering seriously distorted and variable-frequency utility conditions. The proposed synchronization algorithm can suppress the negative sequence utility voltage at fundamental frequency and high-frequency harmonic components effectively, and lock the positive sequence phase at fundamental frequency accurately. Moreover, a frequency adaptation algorithm is also proposed for applications where large frequency variations are often expected. Finally, digital simulation and experimental results both prove the feasibility of the proposed phase-locked method. The introduced synchronization method provides higher degree of immunity and insensitivity to harmonics and other types of pollutions in the utility when used to synchronize inverters.

Keywords: positive sequence; phase-locked loop; PI control; adaptation control; grid-connected inverter.

1 Introduction

As the energy demand and environmental problems increase, the renewable energy sources such as solar energy and wind energy have become very important as an alternative to the conventional fossil energy sources [1, 2]. While the distributed power generation units supply power to the grid, they also bring extra pollutions into the grid if the grid-connected inverters utilize inaccurate phase information of the utility voltages to synchronize with the utility grid. With the development of power electronics, more and more non-linear loads are connected to the electric networks. Therefore, distortions and transients such as harmonics, frequency variations and phase shifts often occur to the grid [3,4]. Moreover, it is reasonable to expect that the level of pollution will increase in the future. Obviously, the accurate phase angle information of utility voltage is very essential to grid-connected inverters. For ensuring the highest transmission efficiency of generated power, it is necessary for unitary power factor control to detect the positive sequence component of utility voltage at fundamental frequency. Thus, synchronization algorithms are of great importance in the control of grid-connected inverters as an integral part of the distributed power generation units [5,6]. Various synchronization techniques have been proposed in literatures. The zero crossing detection methods [7,8], the space-vector filtering (SVF) method [9], the artificial neural networks (ANN) method [10], the recursive weighted least-squares estimation (WLSE) algorithm [11], the discrete Fourier transform (DFT) and its modifications [12], the method based on the concept of adaptive notch filtering (ANF) [13], the Kalman filtering technique [14], the frequency-locked loop (FLL) method [15], three-phase open-loop phase-locked method [16], and the phase-locked loop (PLL) based on algorithms [17, 18,19,20,21,22,23,24,25] are among the existing synchronization techniques.

This paper incorporates the merits of the three-phase open-loop and closed-loop phase-locked method, and puts forward a new closed-loop phase-locked method with frequency adaptation function for three-phase grid-connected inverters. The proposed PLL demonstrates superior performances in terms of synchronization signals even under the conditions of harmonics, frequency variations, phase shifts and unbalance that exist in the utility voltages used as the basis of synchronization. In addition, the salient feature of the proposed PLL is the

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simplicity of structure which renders itself for digital implementation.

2 Conventional closed-loop phase-locked algorithm

A PLL is a nonlinear closed-loop feedback control system which synchronizes its output signal in frequency, as well as in phase, with an input signal. A closed-loop synchronization method operates based on a closed-loop structure which is regulating an error signal to zero. The implementation of a typical three-phase PLL in conformity with the inverter system applications is based on synchronous reference frame transformation. The basic structure of three-phase PLL is shown in Fig. 1.

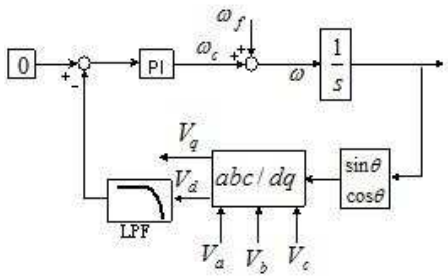

Fig. 1: Block diagram of three-phase PLL

Usually, a three-phase PLL control system is capable of transforming the utility voltage vectors into d-q synchronous rotational coordinates by two transformation matrixes.

$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} = T_{\alpha\beta/dq} * T_{abc/\alpha\beta} \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \tag{1}$$

Where $T_{abc/\alpha\beta}$ is Clark transformation matrix, $T_{\alpha\beta/dq}$ is Park transformation matrix.

$$T_{abc/\alpha\beta} = \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \tag{2}$$

$$T_{\alpha\beta/dq} = \begin{bmatrix} cos\theta_p & sin\theta_p \\ -sin\theta_p & cos\theta_p \end{bmatrix} \tag{3}$$

Assuming the utility voltage vectors as positive sequence fundamental components and substituting (2) and (3) into (1), formula (1) can be simplified as

$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} = \frac{3V_m}{2} \begin{bmatrix} sin(\theta - \theta_p) \\ -cos(\theta - \theta_p) \end{bmatrix} \tag{4}$$

Where V_m is the amplitude of positive sequence fundamental voltage, θ is the actual phase of utility voltages, θ_p is the estimated phase angle.

The ultimate aim of PLL control system is locking the estimated phase value of utility voltages to its actual value. The design of three-phase PLL is based on the small signal analysis in which $sin(\theta - \theta_p)$ is approximated by $(\theta - \theta_p)$. The voltage component V_d in synchronous rotational coordinates is regulated to zero using a PI controller. By integrating with its output value, the synchronous phase angle is acquired.

A desirable closed-loop system should provide both fast tracking ability and high phase-locked accuracy. Conventional three-phase PLL systems use low-pass filters (LPF) to reduce the impact of harmonics after the extraction of d-axis component. Lower cut-off frequency of the low-pass filter causes lesser distortions in the estimated phase angle. However, this results in a poor dynamic performance. So, a trade-off should be made between the two features. Furthermore, if the three-phase utility voltage is seriously polluted, it will be impossible to acquire the accurate phase information of the positive sequence utility voltage at fundamental frequency only depending on the regulation of cut-off frequency. Thus, the three-phase closed-loop system should be redesigned in consideration of heavy pollutions such as harmonics, frequency variations, phase shifts and unbalance that usually exist in the utility voltages.

3 New closed-loop phase-locked algorithm

Based on the theory of symmetrical components [26], the positive sequence components of three-phase utility voltages can be obtained as follows

$$\begin{bmatrix} V_a^+ \\ V_b^+ \\ V_c^+ \end{bmatrix} = T_{pseq} \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \tag{5}$$

Where $T_{pseq} = \frac{1}{3} \begin{bmatrix} 1 & \partial & \partial^2 \\ \partial^2 & 1 & \partial \\ \partial & \partial^2 & 1 \end{bmatrix}$, $\partial = e^{j\frac{2}{3}\pi}$.

In order to eliminate the high-frequency harmonic components in the extracted positive sequence utility voltages, an effective way is to transform the extracted components into $\alpha - \beta$ stationary coordinates.

$$\begin{bmatrix} V_\alpha^+ \\ V_\beta^+ \end{bmatrix} = M_1 \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} e^{-j\frac{\pi}{2}} - M_2 \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} e^{\pi} \tag{6}$$

Where $M_1 = \frac{1}{3} \begin{bmatrix} 0 & -\frac{\sqrt{3}}{2} & \frac{\sqrt{3}}{2} \\ 1 & -\frac{1}{2} & -\frac{1}{2} \end{bmatrix}$, $M_2 = \frac{1}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}$.

For the formula (6), the operator $-j\frac{\pi}{2}$ can be implemented with a filter which is designed to provide unit gain and realize -90^0 phase shift at the fundamental

frequency. Likewise, the operator $j\pi$ can realize -180^0 phase shift by employing the two identical filters in series. Due to the harmonics in the utility voltages which corrupt the synchronization signals, this paper considers the second-order low-pass filter shown in the formula (7) to reduce the harmonics as well as to implement the -90^0 and -180^0 phase shift at the fundamental frequency without any distortion as required to obtain the positive sequence components and eliminate harmonics synchronously. The specified transfer function of the second-order LPF in the Laplace domain is expressed as:

$$LPF = \frac{\omega_n^2}{S^2 + \omega_n S + \omega_n^2} \tag{7}$$

Where ω_n is the natural angular frequency that should be equal to the grid fundamental angular frequency.

The Bode plot of the filter is shown in Fig. 2. It is obvious to see that the filter shows itself as unit gain and -90^0 phase shift at 50Hz. In addition, high-frequency harmonics are significantly reduced. For instance, the second harmonic is attenuated to -11.2 dB, the third harmonic, -18.7 dB and the fifth harmonic, -27.8 dB at the output of the second-order LPF.

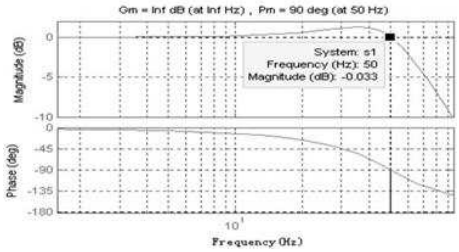

Fig. 2: Bode plot of the second-order LPF

The proposed three-phase PLL structure is shown in Fig. 3. The polluted three-phase utility voltage is transformed into - stationary coordinates. In this way, the feedback loop acquires the positive sequence components and attenuates the high-frequency harmonics synchronously. In addition, the conventional integral is replaced by a sine table ranging from 0^0 to 360^0 which makes the proposed synchronization method more convenient for digital implementation.

4 Frequency adaptation algorithm

In stiff grids, the frequency variation in the considered algorithm is not a concern, but in most countriesthe frequency of grid terminal nodes is often variable. For example, the utility companies usually provide a permissive utility voltage with frequencies variation

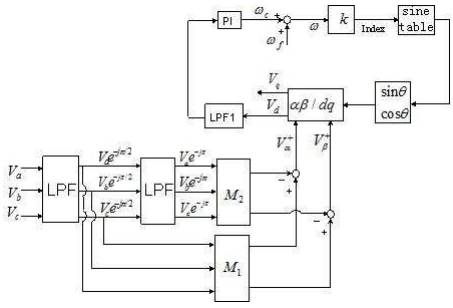

Fig. 3: Block diagram of the new three-phase digital PLL

between 5 Hz, as recommended by AS4777 in Australia. In case of the presence of large frequency variations in the utility grid, the parameter of the second-order filter must be updated in accordance with the fundamental angular frequency in real time. Therefore, a feasible frequency adaptation algorithm should be put forward so as to broaden the range of applications of the proposed synchronization method to weak grid. On the assumption that the output signals of the PLL $sin\theta$ and $cos\theta$ act as the input signals of an extra second-order LPF, the output signals of the LPF can be expressed as $\lambda sin(\theta - \sigma)$ and $\lambda cos(\theta - \sigma)$ respectively. If the natural frequency of the filter ω_n is equal to the grid frequency, the amplitude λ is 1. However, if the natural frequency is bigger than the grid frequency, $\lambda > 1$, which means that the LPF amplifies the input signals. Else, the filter shows attenuation function when the natural frequency is smaller than the fundamental frequency of the utility voltage, namely, $\lambda < 1$. Then, a simple trigonometric equation $(\lambda sin(\theta - \sigma))^2 + (\lambda cos(\theta - \sigma))^2 = \lambda^2$ can be used as feedback. Defining a frequency adaptation function $f(\hat{\omega}_n, \omega) = \lambda^2$, if the feedback value $f(\hat{\omega}_n, \omega) > 1$, it indicates that the evaluated angular frequency of the filter $\hat{\omega}_n$ is bigger than the grid fundamental angular frequency. On the other hand, if $f(\hat{\omega}_n, \omega) < 1$, it indicates that $\hat{\omega}_n$ is smaller than the grid fundamental angular frequency. Then, the error $1 - \lambda^2$ can be used to estimate the grid fundamental angular frequency, using an integral controller, as shown in Fig. 4.

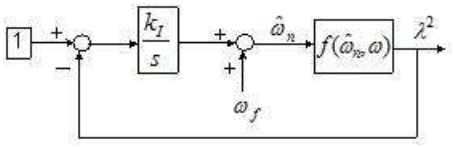

Fig. 4: Frequency adaptation algorithm

Further, the frequency adaptation algorithm can be induced to the following relationship between the estimated frequency and grid fundamental frequency.

Then, the estimated angular frequency $\hat{\omega}_n$ will be updated if the frequency variation occurs to the utility voltage.

$$\hat{\omega}_n = \omega_f + \frac{k_I}{s}(1 - f(\hat{\omega}_n, \omega)) \tag{8}$$

Where the grid nominal frequency ω_f is only a feed-forward component, and k_I is the integral coefficient for the frequency adaptation feedback loop. Furthermore, the effective frequency adaptation range is set within 5 Hz. The block diagram of the new all-digital closed-loop phase-locked method with frequency adaptation function for the three-phase grid-connected inverters is shown in Fig. 5.

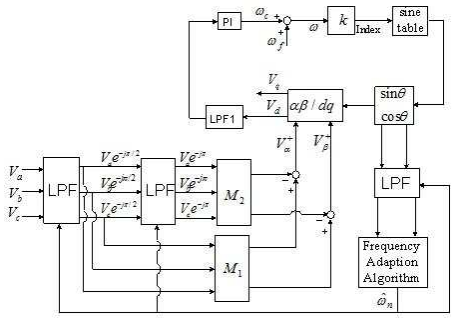

Fig. 5: Block diagram of the proposed PLL with frequency adaptation algorithm

By means of a transfer coefficient, that is,k, the estimated angular frequency is transformed into the index value of the sine table listed in digital program. The transfer coefficient is defined as:

$$k = \frac{180}{\pi} * \frac{N}{360} * T_s \tag{9}$$

Where N is the number of specified sine values in the sine table, T_s is the sampling period.

In order to reduce the coupling degree between the proposed PLL feedback control and frequency adaptation control, the bandwidth of phase-locked loop should be far larger than that of the adaptation algorithm. The phase-locked PI controller calculates every one sampling period,while the frequency adaptation integral controller calculates every thirty sampling periods.

The digital delayed effect of sampling and calculating may degrade the stability of the proposed PLL control system. Therefore, the delay $(e^{-\Im})$ should be taken into account for the design of the closed-loop PI control. In order to give attention to the stability as well as fast tracking ability of the PLL control system, the feedback control loop should be designed to reach the steady state within five sampling periods for the unit step signal. Five dynamic curves for different PI parameters are shown in Fig. 6. Where the digital proportional and integral parameters corresponding to the curves from 1 to 5 are (1.8,0.003), (0.9,0.002), (1.1, 0.006), (0.5,0.002) and (0.3,0.001) respectively. The PI parameter (1.1, 0.006) is adopted in the next simulation and experiment so as to validate the effectiveness of the proposed PLL control system.

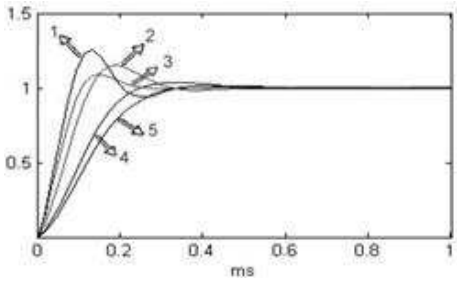

Fig. 6: Curves of unit step response for different PI parameters

5 Simulation results

Performance of the proposed PLL method is evaluated by means of a number of simulations. Simulations based on C programming language are implemented by the S-function of MatlabSimulink. The key PLL parameters are shown as follows:

$T_s = 50 * 10^{-6}s, N = 720, k = 0.00573, LPF1 = \frac{850}{s+850}, k_I = 1.2$

To show the promising behaviors of the proposed synchronization method, several operation conditions are considered in the following simulations.

5.1 Harmonic distortion simulation

Usually, the odd harmonic contents in the utility voltage are high, while even harmonics are few and can be neglected. Hereby, the three-phase utility voltages in the presence of heavy harmonic pollution are shown as:

$$\begin{cases} V_a = 411sin(\omega_0 t) + 100sin(3\omega_0 t) + 100sin(5\omega_0 t) + \\ \quad 100sin(7\omega_0 t) + 100sin(9\omega_0 t) + 100sin(11\omega_0 t) \\ V_b = 311sin(\omega_0 t - \frac{2pi}{3}) + 100sin(\omega_0 t + \frac{2pi}{3}) + \\ \quad 100sin(3\omega_0 t) + 100sin(5\omega_0 t - \frac{2pi}{3}) + \\ \quad 100sin(7\omega_0 t - \frac{2pi}{3}) + 100sin(9\omega_0 t) + \\ \quad 100sin(11\omega_0 t + \frac{2pi}{3}) \\ V_c = 311sin(\omega_0 t + \frac{2pi}{3}) + 100sin(\omega_0 t - \frac{2pi}{3}) + \\ \quad 100sin(\omega_0 t) + 100sin(5\omega_0 t - \frac{2pi}{3}) + \\ \quad 100sin(7\omega_0 t + \frac{2pi}{3}) + 100sin(9\omega_0 t) + \\ \quad 100sin(11\omega_0 t - \frac{2pi}{3}) \end{cases} \tag{10}$$

As shown in Fig.7 and Fig.8, the THD of the sinusoidal synchronous signals for the proposed algorithm is low. The THD are 0.15% at the fundamental frequency of utility voltage 50Hz, and the THD are 0.21% at 52Hz

5.2 Three-phase voltage unbalance simulation

Under power faulty conditions, the three-phase utility voltages with different DC offset components and negative sequence component at fundamental frequency are shown as:

$$\begin{cases} V_a = 411sin(\omega_0 t) + 100 \\ V_b = 311sin(\omega_0 t - \frac{2pi}{3}) + 100sin(\omega_0 t + \frac{2pi}{3}) + 60 \\ V_c = 311sin(\omega_0 t + \frac{2pi}{3}) + 100sin(\omega f_0 t - \frac{2pi}{3}) + 20 \end{cases} \quad (11)$$

Fig. 9 shows the phase comparison between the A-phase positive sequence fundamental component and the amplified sinusoidal synchronization signal for the proposed PLL method. The THD of the sinusoidal synchronization signal is 0.08%. The waveforms 1 and 2 stand for the A-phase positive sequence fundamental component and the amplified sinusoidal synchronization signal, respectively.

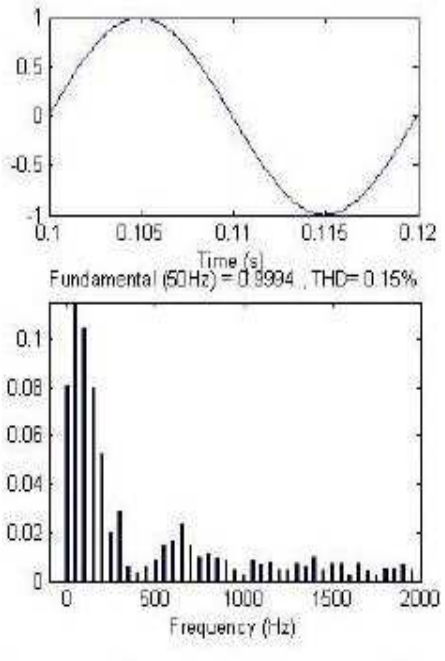

Fig. 7: Phase-locked precision of the proposed algorithm at frequency 50Hz

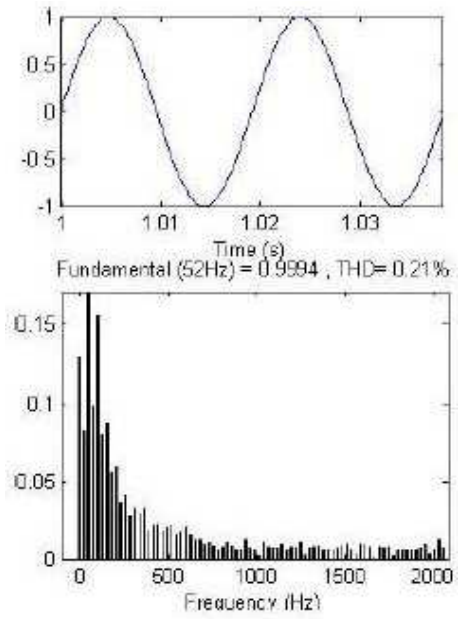

Fig. 8: Phase-locked precision of the proposed algorithm at frequency 52Hz

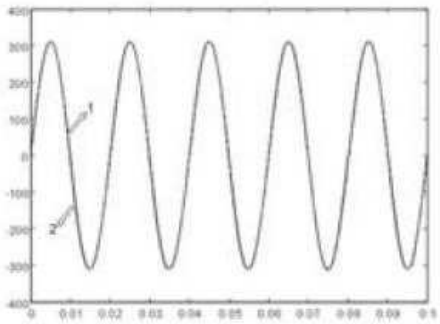

Fig. 9: Phase comparison between positive sequence fundamental voltage and amplified sinusoidal synchronization signal for the proposed PLL

5.3 Frequency and phase jumping simulation

In Fig. 10, a transient phase error is generated when a fundamental frequency step of 5 Hz occurs to the three-phase utility voltage at 20ms. The phase error will come close to zero again in about two utility cycles for the proposed phase-locked method with the frequency adaptation function. When a fundamental phase jump of 20 degrees occurs to the input signal at 20ms, the phase error dynamic response is shown in Fig. 11. A transient phase error with a peak of 20 degrees is observed and it will reach the steady state in a few utility cycles for the proposed phase-locked method. In the two figures, the

waveform A indicates the A-phase positive sequence fundamental component, and the waveform B indicates the A-phase polluted utility voltage. The phase error curve 1 shows the tracking ability of the proposed PLL. By results, the phase-locked algorithm in this paper shows the good dynamic performance.

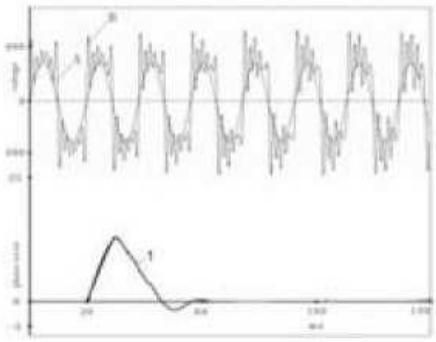

Fig. 10: Phase error dynamic responses when fundamental frequency varying by 5Hz at 20 ms

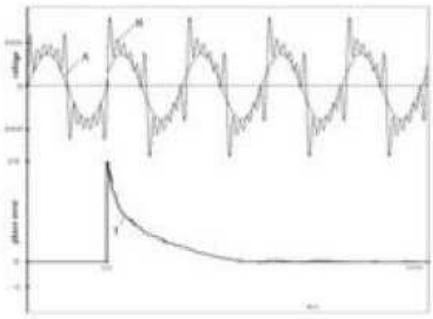

Fig. 11: Phase error dynamic responses when fundamental phase jumping by 20 degrees at 20 ms

6 Experimental results

Performance of the proposed synchronization method is also evaluated by experimenting. The algorithm is programmed in a DSP board TMS320F2812 and implemented in a 10kVA three-phase grid-connected inverter. In order to observe the transient behavior of the recommended frequency adaptation algorithm, the anti-island function of the inverter is disabled and the inverter is not disconnected from grid when the utility is abnormal. The experimental PLL parameters are the same as those of the simulation. The heavy polluted utility voltages are shown as formula (10). Fig. 12 and Fig. 13 show the experimental results about the steady state and transient behavior for the proposed PLL method. In two figures, the waveforms indicate the A-phase polluted utility voltage, the A-phase positive sequence fundamental component and the amplified sinusoidal synchronization signal. For evaluating the startup transient behavior of the PLL, as shown in Fig. 12, it is possible to see a fast transient response, reaching the steady state in less than one utility cycle. At the steady state, the metrical THD of the synchronization signal is 0.19%. The synchronization signal will reach the steady state within two utility cycles when the fundamental frequency varies from 50Hz to 55Hz at the beginning, as shown in Fig. 13.

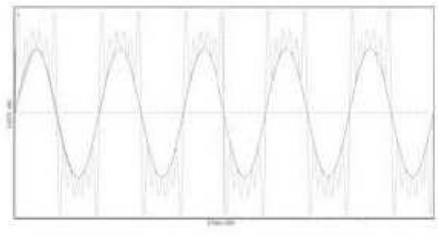

Fig. 12: Dynamic waveforms of the proposed PLL for polluted utility at fundamental frequency 50Hz

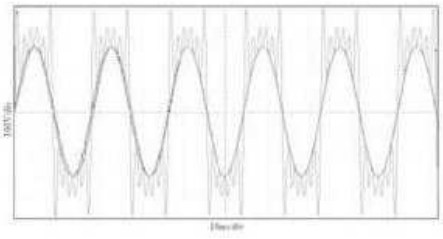

Fig. 13: Dynamic waveforms of the proposed PLL with frequency adaptation function when fundamental frequency varying from 50Hz to 55Hz at 0 ms

7 conclusions

The frequency and phase angle of the grid voltage, which are usually detected by a PLL, are important for the grid-connected inverters. A new closed-loop phase-locked algorithm for three-phase grid-connected inverters has been proposed in this paper. The

synchronization algorithm is provided with a formal closed-loop structure, including a positive sequence extraction module and a frequency adaptation calculating module. Digital simulation and experimental results both show that the proposed PLL has good steady-state and dynamic performances even under the conditions of harmonics, frequency variations, phase shifts and unbalance that exist in the utility voltages.

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Jifeng Guo received the PhD degree in 1990 from Zhejiang University. Since 1998 he has been a professor at the College of Electrical Engineering, Zhejiang University. His main interests are in ultrasonic motors, vibration analysis and control, space robotics and renewable energy systems. He is a member of the editorial board of the Chinese Journal of Astronautics.