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Analog and RF Performance Analysis of 22nm Modified Source/Drain Dual Gate FDSOI MOSFET

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Abstract: In this paper, 22nm FDSOI MOSFET having Modified Source/Drain with Dual Gate has been analyzed. This device, not only provides higher ON current but it has also a lower leakage current in order of pA. With the help of Dual Gate (DG) electrical characteristics and Short Channel Effects improved. Analysis parameters like Drain Induced Barrier Lowering (DIBL), Subthreshold Swing, Threshold roll-off, Carrier Concentration, Gate to drain Capacitance, Gate to Source Capacitance, cut-off frequency, Conduction and Valence Band Banding are analyzed using high-k spacers.
Keywords: FDSOI MOSFET, modified Source/Drain, intrinsic gain, trans-conductance, cut-off frequency.

1. Introduction

To improve the efficiency of transistors in accordance with the scaling of device is becoming challenging for manufacturers and researchers. Manufacturing cost is also a very important factor in the electronics industry with performance, and as ITRS shows that technology changing within the decade. And due to scaling of devices structure complexity arise, and various types of Short Channel effects (SCEs) come into existence like Drain induced barrier lowering (DIBL), Threshold Voltage roll-off, Subthreshold swing lowering, Gate induced barrier lowering (GIBL) and leakage currents [1-4]. R.Carter *et al.* shows how the 22nm FDSOI technology can be used for different applications like RF, Mobile and Internet-of-Things (IOT) [5]. It also reduces the device complexity compared to FinFET 14/16nm technologies. Yamada et al. proposed channel engineering [6], Nilesh *et al.* came up with modified source engineering [7], work function difference engineering brought up by Sandeep *et al.* [8]. Pradhan *et al.* explains the impact of high-k dielectric on RF and analog application. Gate stack method reduces gate-tunneling current and provides better electrical performance to some extent [9]. Nowadays analog and RF are the fields where research is required and different parametric analysis like intrinsic gain, noise figure and cut-off frequency has to be done [10-15].

To encounter all the issues related to the scaling, we have proposed 22nm Modified Source/Drain Dual Gate FDSOI MOSFET. Advantage of FDSOI is well known, i.e. high switching ratio, higher drive current, low leakage, low power application, high trans-conductance and higher I_{on} to I_{off} ratio [16]. Current research is now a mixer of analog and digital so to fulfill the requirement, the device should perform under analog domain also. Moreover, the analog trans-conductance, cut-off frequency, and intrinsic gain are the parameters to analyze. Mishra et al. proposed the modified source FDSOI at 50 nm to enhance the performance of the device in terms of higher drive current, high switching ratio and low leakage current [17]. Y.S. Chauhan *et al.* has explained physical insight, how substrate can affect the frequency behavior on trans-conductance in ultra-thin body FDSOI MOS devices [18]. Himanshu *et al.* has introduced both drain and source engineering [19-20], Narendra *et al.* has proposed asymmetric design using epitaxial source double gate MOSFET [21].

2. Device Structure and Specifications

Device structure is shown in Figure 1. This device is taken in symmetrical dimensions to moderate design complexity. Malviya *et al*. has proposed a similar structure using 50nm and 22nm gate length [22-23]. Source and Drain, both are engineered with two different doping profiles. The upper part of both regions is highly doped with $2x10^{20}/cm^3$ and lower part of the region is doped with $1x10^{18}/cm^3$. In the device dual gates are used for a better channel control and to achieve a higher drive current. Channel is 22 nm long, and oxide thickness t_{ox} is varied from 2nm to 1nm. Gate

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metal engineering, with different work function ϕ(s) between 4.1-4.7 eV, is used to find different threshold voltages V_{th} and subthreshold swing (SS). With Different structures, different high-k dielectrics as SiO_2, Si_3N_4, Al_2O_3, HfO_2 and TiO_2 are used and shown in table 2. High-k dielectric increases the gate capacitance and reduces the leakage current which enhances the drive current. Table 3 shows the different work function gate metals that can be used to control the hot carrier effect and V_t roll-off. All of the different gate materials are used with the common high-k dielectric TiO_2. Device thickness is also kept on 1 nm. Drain potential is set to 0.8V with variable gate potential from 0-0.8V, according to international technology road map of semiconductor (ITRS) for 22 nm gate length [24]. Thickness variation is also done with a higher work function metal gate because oxide thickness is also a big challenge with the scaling of the device, and below 2 nm it can increase the power consumption due to tunneling.

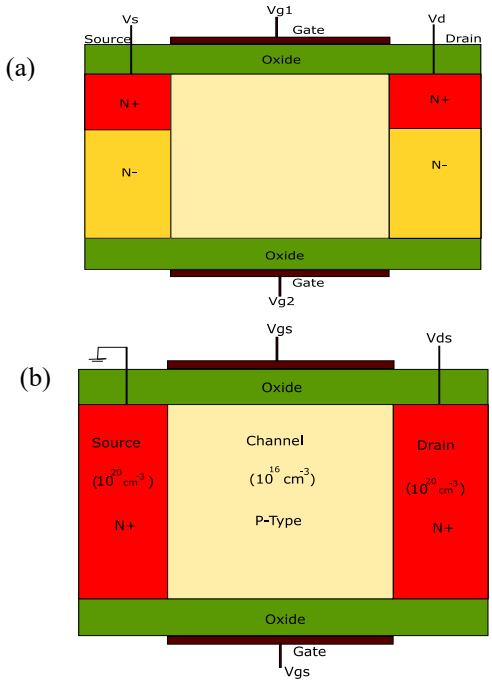

Figure 1. (a) Device structure of the proposed device with oxide thickness (t_{ox}) = 1 nm, channel length (L) = 22nm, drain and source Side N^+ doping=10^{20} cm^{-3} and N^- doping = 10^{17} cm^{-3}, (b) DG-MOSFET [9].

Table 1. Device Specification for the proposed device.

S. N.	Parameters	MSMD 22nm FDSOI
1.	Gate length	22nm
2.	T_{ox}	1nm
3.	Substrate doping	1e16 cm^{-3}
4.	Source region doping n+	1e20 cm^{-3}
5.	Source region doping n-	1e17 cm^{-3}
6.	Drain region doping	1e20 cm^{-3}
7.	Work function of Gate	4.77eV
8.	Gate voltage	1.1 volts
9.	Silicon film thickness	12nm
10.	Silicon Substrate	5nm

Table 2. Dielectric constants for different high-k dielectrics.

S. N.	Device	Dielectric Material	Dielectric Constant
1.	D1	SiO_2	3.9
2.	D2	Si_3N_4	7.5
3.	D3	Al_2O_3	10
4.	D4	HfO_2	30
5.	D5	ZrO_2	50
6.	D6	TiO_2	80

Table 3. Work function variation with constant oxide thickness and dielectric constant.

S. N.	Device	Gate Work Function	Oxide
1.	D7	4.35	TiO_2
2.	D8	4.5	TiO_2
3.	D9	4.7	TiO_2

3. Result Analysis

For the device to work as a good amplifier, its gain should be higher, and to work as a fast switching device, its i_{on} to i_{off} ration should be large. And with this device, we have achieved better results for both cases. The device with two different biasing potential, V_{DS}=0.1V and V_{DS}=0.8V, have been analysed. In the device, we used 6 different high-k dielectrics and named all the devices from D1 to D6, and all of the different device characteristics are compared to obtain a suitable operating condition in all conditions. D7, D8 and D9 devices are analysed at different work function, and corresponding threshold voltage variation is observed. Analog and RF performance are valued for the device D6, because device D6 has, comparatively, better i_{on} and i_{off} currents and I-V characteristics, so we have chosen D6 for the parametric analysis. Figure 2 is a I-V characteristic between drain current and gate to source voltage (V_{GS}). Drain current is defined in logarithmic values on y-axis and gate voltage is on x-axis. As we increase the dielectric constant the value of Drain Current, i.e., drive current is increasing and on other hand the off current i.e. leakage current is decreasing also. Figure 3 shows the I-V characteristic between Drain Current and Drain Voltage (V_{DS}) at different gate biasing voltages V_{GS}=0.4V, V_{GS}=0.6V and V_{GS}=0.8V. When the gate voltage is below the threshold voltage then device is in the off state, and no current flows, and as the gate voltage increases to 0.8 the device becomes on, and the current starts flowing from drain to source. Figure 4 is a comparison between subthreshold slop of different devices at different dielectric constants. Form the graph, it is clear that the Subthreshold

Slop (SS) for high-k dielectric is less then low-k dielectric constant material. For TiO_2, it is minimum, and for SiO_2, it is maximum. Subthreshold is an important parameter in the short channel effects, and minimum Subthreshold cannot be less than 60mV/decade, and it is given by the equation 1 [25]. Subthreshold should be minimal fast turn off and turn on of the device [25]. Device 1(b) has a V_{DD}=1V, and the high-k used is Ta_2O_5.

$$SS = \left[\frac{\partial\, log_{10}(I_d)}{\partial V_{GS}}\right]^{-1} \quad (1)$$

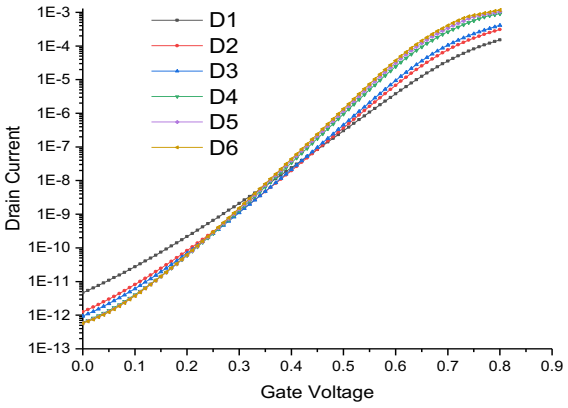

Figure 2. Drain current to gate voltage I-V characteristics with different dielectrics at V_{DS}=0.8 and t_{ox}=1nm.

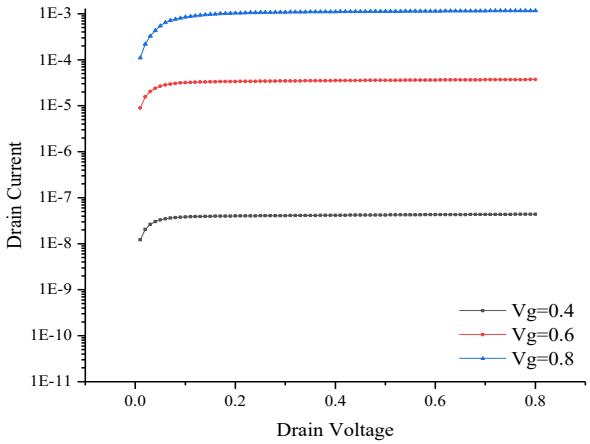

Figure 3. Drain current and drain voltage characteristics at V_{GS}=0.4, V_{GS}=0.6 and V_{GS}=0.8V.

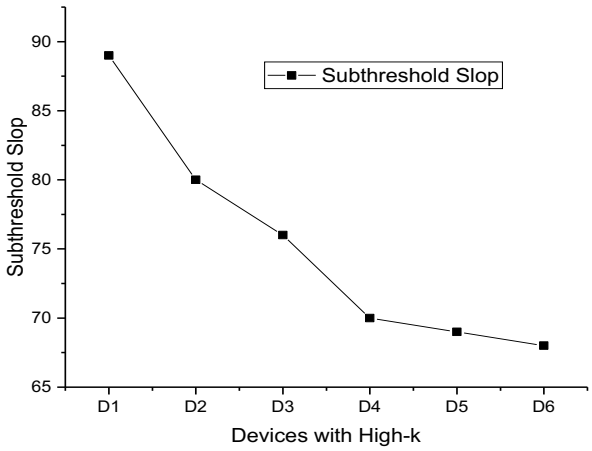

Figure 4. Subthreshold slop with different high-k dielectrics at V_{DS}=0.8V.

Threshold Voltage is a cut off voltage for the device from where the device starts operating. Figure 5 is a comparison of the threshold voltages (V_{th}) at different values of dielectric constant. From the graph, it is clear that there is not a significant effect on threshold voltage of the proposed device, and it is approximately constant though the device variation. All the threshold voltages are calculated on the same biasing conditions, V_{DS}=0.8V. Leakage current, i.e., off state current (I_{off}) is shown in Figure 6 and Drive current, i.e., on current (I_{on}) is measured in ampere at the saturation of the device, and shown in Figure 7. Both graphs are compared for all devices, and it is found that for the larger values of dielectric constant, not only the on current is increasing, but also the off current is decreasing simultaneously. The lowest value of leakage current is in the order of pA for D6, it means that the leakage current is reduced at a large scale, as compared to D1. For any switching device, its I_{on} to I_{off} ratio should be large as much as possible, and it is shown in Figure 8 at V_{DS}=0.8V. In the proposed structures, device D1 has lowest value of a ratio, and as we move to higher value of dielectric then the ratio increases and for the device D6, it is at maximum, and it is $2e10^9$.

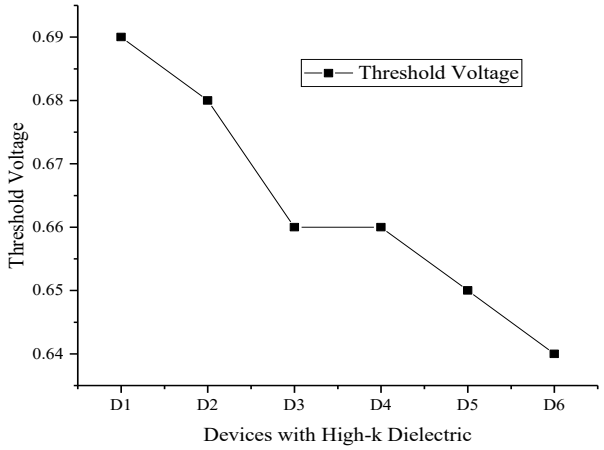

Figure 5. Threshold voltage under different high-k dielectrics at V_{DS}=0.8V.

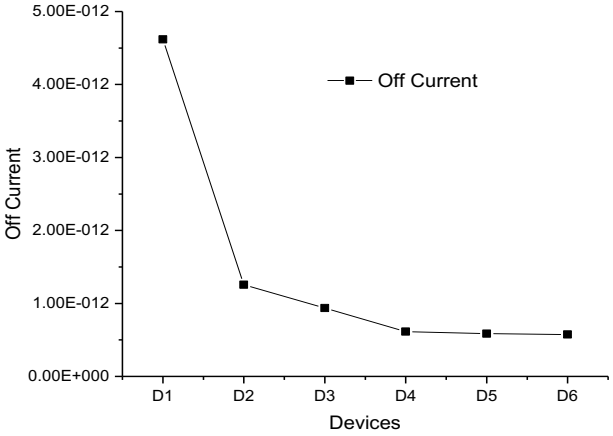

Figure 6. Off current under different high-k dielectrics at V_{DS}=0.8V.

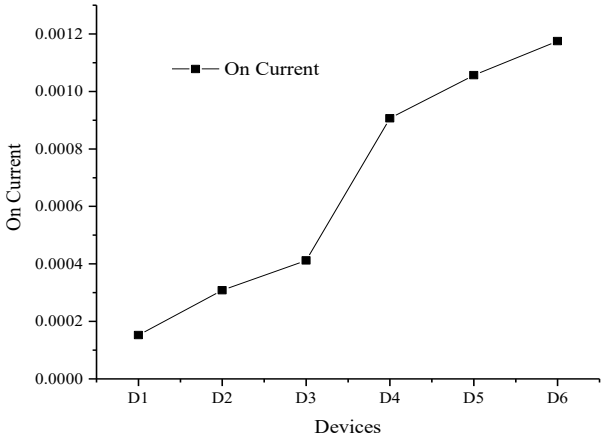

Figure 7. On current under different high-k dielectrics at V_{DS}=0.8V.

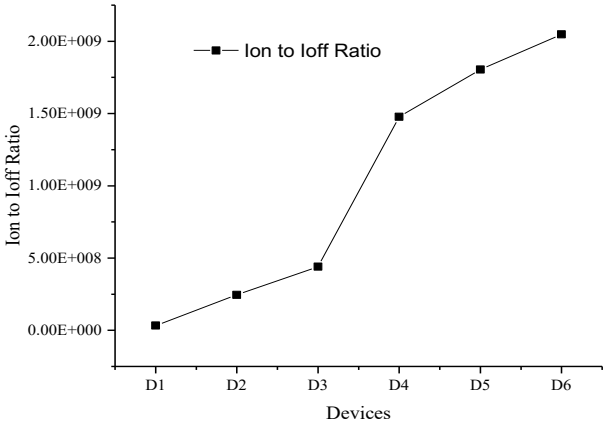

Figure 8. On current to Off current ratio under different high-k dielectrics at V_{DS}=0.8V.

Trans-conductance (g_m) is a parameter that defines how much the output current changes with respect to the input voltage that is expressed in equation 2, and they are compared in Figure 9. From D1 to D6, it increases by increasing the gate voltage V_{GS}. For D1, it shows less change in the output current with a change in input voltage, but it is the maximum in case of D6. Output trans-conductance (g_d) is defined by equation 3. It is nothing but the variation of output current i_d with the output voltage V_{DS}, and it is compared for the device D6 at V_{DS}=0.4V, V_{DS}=0.6V and V_{DS}=0.8V in Figure 10. As we move to higher values of V_{DS}, it increases because, then only the device that starts conducting before threshold voltage it is in the off state. Both g_m and g_d describe the analog performance of the device. For a larger value of gain A_v, the trans-conductance g_m should be large as shown in equation (4) [25]. Figure 11 is an energy band distribution at drain voltage V_{DS}=0.1V. In the off state device, band structure, as shown is similar to what we expect. There is not much difference in the energy levels of the source to drain side. Band gap E_g found for the proposed device, at V_{DS}=0.1V, is 1.1 eV. For V_{DS}=0.8V, the energy band structure is shown in Figure 12. When we apply the drain potential, the conduction band level shifts towards the valence band energy level, and electrons, get sufficient amount of energy to cross the barrier, and the drain current starts increasing. At some value of the V_{DS}, the conduction band level, gets in front of the valence band level and electrons get tunnelled to the drain side. And above that, the level device enters into the degenerated field. Figure 11 is an energy band distribution at drain voltage V_{DS}=0.1V. In the off state device, band structure, as shown, is similar to what we expect. There is not much difference in the energy levels of the source to drain side. Band gap E_g found for the proposed device, at V_{DS}=0.1V, is 1.1 eV. For V_{DS}=0.8V, the energy band structure is shown in Figure 12. When we apply the drain potential, the conduction band level shifts towards the valence band energy level, at electrons get sufficient amount of energy to cross the barrier and the drain current starts increasing. At some value of V_{DS}, the

conduction band level gets in front of the valence band level and electrons get tunnelled to the drain side. And above that, the level device enters into the degenerated field. Due to electric field E, electrons experience some force and get aliened in the opposite direction of the electric field and starts moving with a velocity.

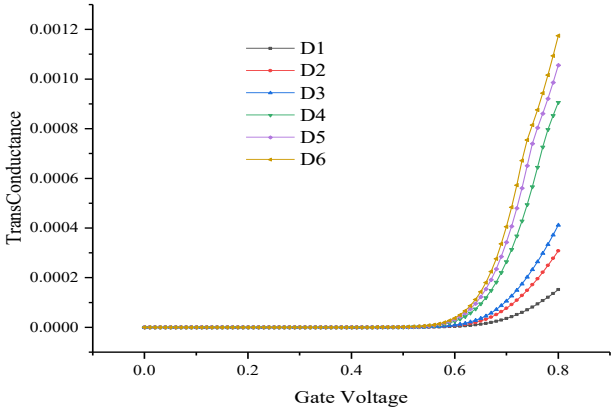

Figure 9. Trans-conductance, g_m(S) under different high-k dielectrics at V_{DS}=0.8V.

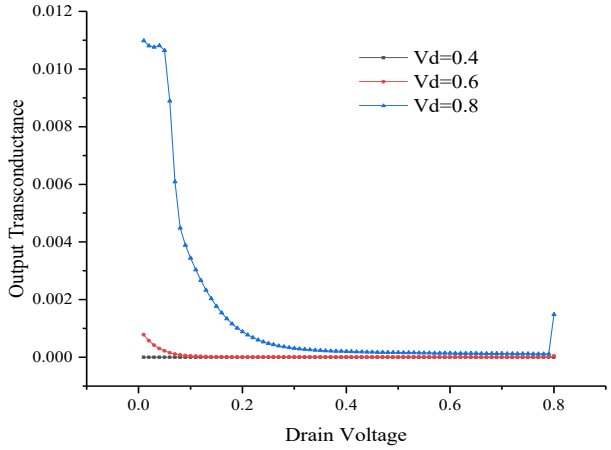

Figure 10. Output Transconductance, g_d (S) under different high-k dielectrics, other parameters are oxide thickness (tox)=1nm, High-k=TiO_2 and L=22nm at V_{DS}=0.8V.

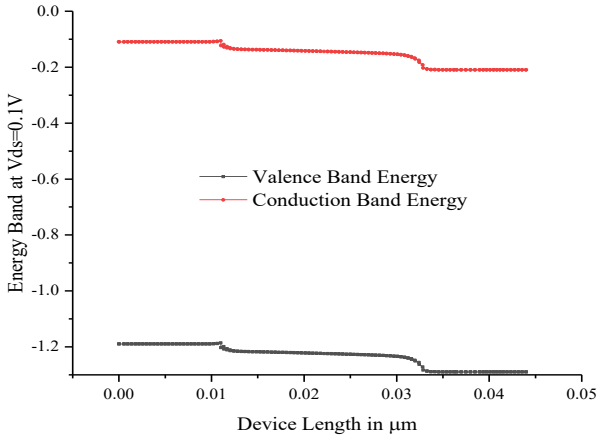

Figure 11. energy bad gap comparison of valance band and conduction band from end to end of device. Other Parameters are Drain Voltage (V_{DS})=0.1V, oxide thickness (t_{ox})=1nm, high-k=tio_2 and channel length (L)=22nm.

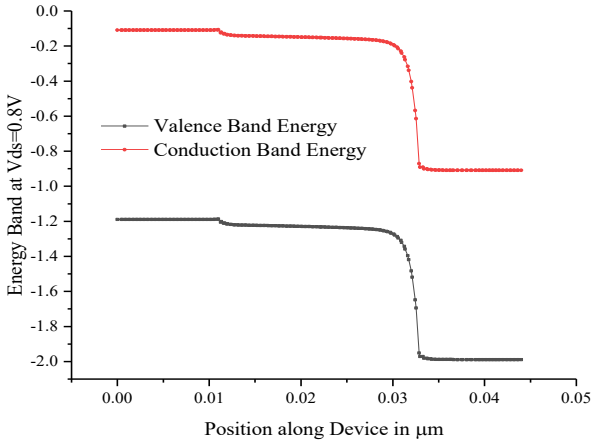

Figure 12. Energy bandgap comparison of valance band and conduction band from end to end of the device. Other parameters are drain voltage (V_{DS}) =0.8V, oxide thickness (tox) =1nm, High-k=TiO_2 and channel length (L) =22nm.

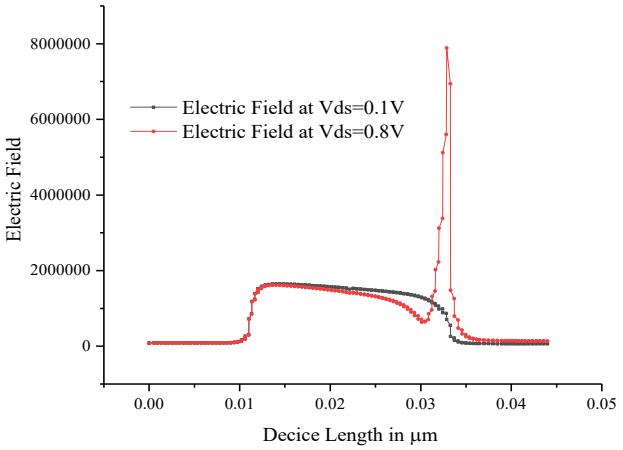

Figure 13. Electric field comparison at different drain bias potential (V_{DS}) from end to end of the device. Other parameters are oxide thickness (t_{ox})=1nm, High-k=TiO_2 and channel length (L)=22nm.

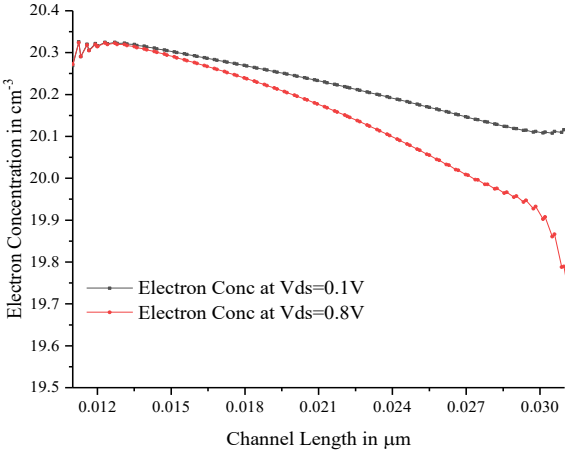

Figure 14. Electron concentration of the proposed device from end to end of the channel. Other parameters are Drain

Voltage (V_{DS}) =0.1V, oxide thickness (t_{ox}) =1nm, high-k=tio$_2$ and channel length (L) =22nm.

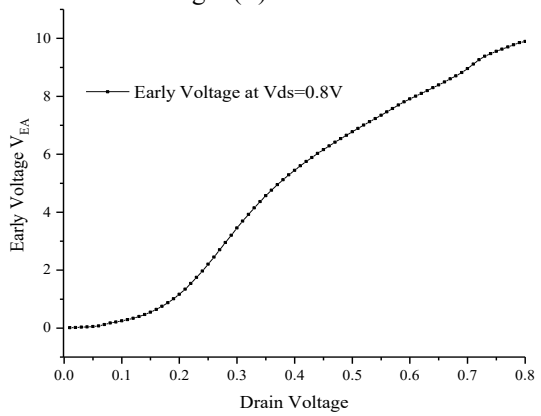

Figure 15. Early voltage (V_{EA}) as a function of Drain Voltage (V_{DS}). Other Parameters are V_{DS}=0.8V, Oxide thickness (t_{ox})=1nm, High-k=TiO_2 and channel length (L)=22nm.

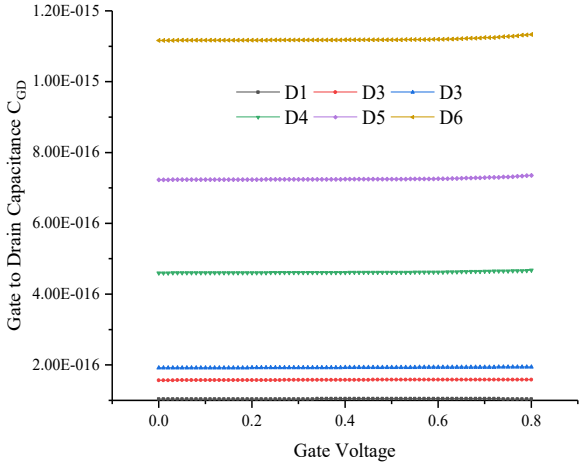

Figure 16. Gate to drain Capacitance (C_{GD}) with the variation of gate to source voltage (V_{GS}) of the proposed device. Other parameters are drain voltage (V_{DS})=0.8V, oxide thickness (t_{ox})=1nm, High-k=TiO_2 and channel length (L)=22nm.

Same electric field is shown in the figure 13 at two different biasing conditions V_{DS}=0.1V and V_{DS}=0.8V. When the device is not on, then the electric field is at a constant level throughout the channel, and as the device gets in the saturation state, the electric field starts decreasing, as we are moving towards the drain region. How electron is distributed along the channel is shown in Figure 14. Electron concentration in cm^{-3} at V_{DS}=0.1V and V_{DS}=0.8V for the device D6 is compared, and it is clear that the concentration of electrons in the off state is less in the channel, and at on state, electron concentration is increased due to the formation of an inversion layer at higher V_{DS} biasing. Early voltage (V_{EA}) is a parameter used in the analysis of analog performance of the device. It is nothing but the ratio of the drain current I_d to the output conductance g_d as shown in the equation (5). For the lower values of g_d, higher is the ratio. Variation of V_{EA} vs drain voltage is shown in Figure 15 at V_{GS}=0.8V. As we increase the value of drain voltage V_{DS}, the value of early voltage increases and at saturation level it reaches 10V.

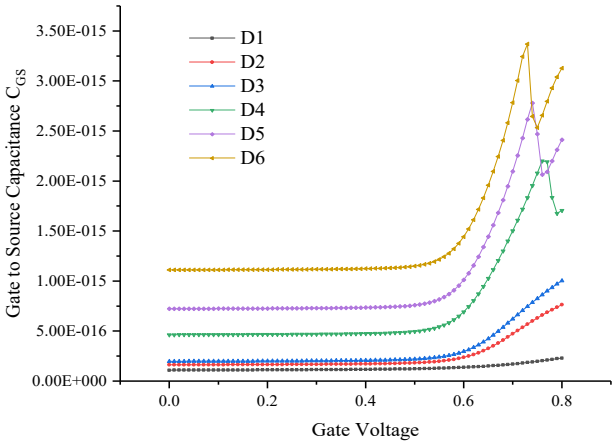

Figure 17.1 Gate to source capacitance (C_{GS}) with the variation of gate to source voltage (v_{gs}) of proposed device. Other Parameters are Drain Voltage (V_{DS}) =0.8V, Oxide Thickness (t_{ox}) =1nm, High-k=TiO_2 and channel length (L) =22nm.

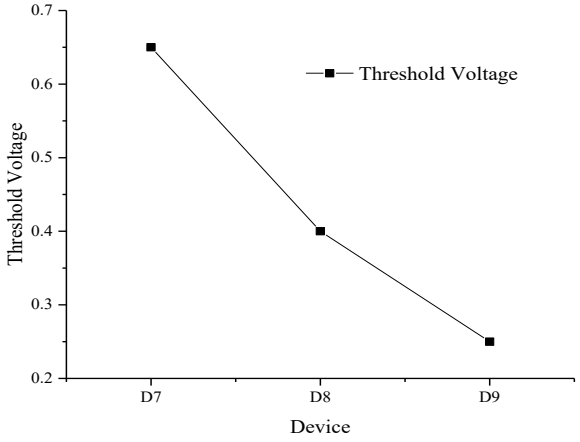

Figure 18.2 Threshold voltage v_{th} variation of devices with the change in the gate metal work function at t_{ox}=1nm V_{DS}=0.8V.

Table 4. Analog and RF performance at t_{ox}=1nm, high-k=TiO_2, V_{DS}=0.8V, V_{GS}=0.8V, channel length=22nm, DG-MOSFET at V_{DS}=0.5, L=22nm, high-k=Ta_2O_5.

RF Parameters	MSMD DG FDSOI 22nm	DG MOSFET 22nm[9]
Gain A_V (dB)	36.44	32.984
g_m(mS)	7.9	2.95
g_d(mS)	0.12	0.06
TGF(V^{-1})	35.68	34.148
f_T (GHz)	3.02	3.86
C_{GS}(fF)	3.3	0.905
C_{GD}(fF)	1.2	0.502
V_{EA}(V)	9.85	7.069
GFP(Hz)	$10.9x10^{12}$	$12.4x10^{12}$
TFP(Hz)	$2.17x10^{12}$	$3.43x10^{12}$
GTFP(Hz)	$79.07x10^{12}$	$58x10^{12}$

Capacitances gate to drain C_{GD} and gate to source C_{GS} in F is shown in Figure 16 and 17, respectively. Gate to drain capacitance is constant with the increase in the gate voltage V_{GS}. It is compared for D1 to D6 different devices at different higk-k. From Figure 16, it is clear that the gate to drain capacitance for the higher value of dielectric is at maximum and increases with high-k. Figure 17 is a comparison of the gate to source capacitance. Until the device is in the off-state, it is constant and as it crosses the threshold, level gate to source capacitance increases with the gate voltage. For device D1 (k=3.9), it is at maximum and increases with the dielectric constant, as shown in the figure. General expression for the capacitance (C) is given by equation (6) [25].

$$g_m = \partial i_d / \partial V_{GS} \quad (2)$$

$$g_d = \partial i_d / \partial V_{DS} \quad (3)$$

$$A_v = g_m / g_d \quad (4)$$

$$V_{EA} = i_d / g_d \quad (5)$$

$$C = (A * \varepsilon_r)/d \quad (6)$$

$$\text{Cut} - \text{off frequency } (f_T) = \frac{g_m}{2\pi(C_{GS}+C_{GD})} \quad (7)$$

$$\text{Gain Frequency Product(GFP)} = \text{gain} * f_T \quad (8)$$

$$\text{Trans} - \text{conductance Product(TFP)} = \frac{g_m}{i_D} * f_T \quad (9)$$

$$\text{Gain Trans} - \text{conductance Product(GTFP)} = A_v * \text{TFP} \quad (10)$$

$$\text{Transconductance generation factor(TGF)} = \frac{g_m}{i_D} \quad (11)$$

Analog and RF analysis on different parameters like gain A_v, g_m, g_d, cut-off frequency (equation 7), gate to source capacitance C_{GS}, gate to drain capacitance C_{GD}, early voltage V_{EA}, gain frequency product GFP (equation 8), trans-conductance frequency product TFP (equation 9), gain trans-conductance frequency product GTFP (equation 10) and trans-conductance generation factor TGF (equation11) are included in Table 4 [25].

4. Conclusions

For the optimization of the proposed device, different high-k dielectric constants are used in the devices D1 to D6. Threshold voltage variation with work function is shown in the devices D7, D8 and D9. As we decrease the work function, the threshold voltage V_{th} decreases consequently. D6 has 669.7% more drive current, leakage current is reduced to 87.57% and I_{on} to I_{off} ratio is increased compared to device D1. Compared to the device DG MOSFET [9], analog and RF performance of MSMD DG FDSOI is analogous. Some parameters like Gain, Early Voltage, trans-conductance generation factor, and gain trans-conductance frequency product has high values, as compared to DG MOSFET [9]. Cut-off frequency and trans-conductance frequency product are lower than DG MOSFET [9]. Trans-conductance generation factor is also close to the ideal value, i.e., $40V^{-1}$ for 60mv/decade subthreshold slope. Subthreshold slope of D6 is also better than the devices. Work function can control the threshold voltage and we can lower the threshold voltage by increasing the value of work function, as shown in Figure 18. We can also use high-k gate stack to achieve more control over the channel and short channel effects. So in the proposed devices, D6 could be the best option for the design of analog and RF circuits.

References

[1] D. J. Frank, R. H. Dennard, E. Nowak, P. M. Solomon, Y. Taur and H. S. P. Wong, Device scaling limits of Si MOSFETs and their application dependencies, *Proceedings of the IEEE,* **89**, 259-288 (2001).

[2] I. Ferain, C. A. Colinge and J. P. Colinge, Multigate transistors as the future of classical metal–oxide–semiconductor field-effect transistors, *Nature*, **479**, 310 (2011).

[3] L. Chang, Y. K. Choi, D. Ha, P. Ranade, S. Xiong, J. Bokor, C. Hu and T. J. King, Extremely Scaled Silicon Nano-CMOS Devices, *Proc. IEEE*, **91**, 1860–1873 (2003).

[4] T. Skotnicki, J. A. Hutchby, T. J. King, H. S. P. Wong and F. Boeuf, The end of CMOS scaling: toward the introduction of new materials and structural changes to improve MOSFET performance, *IEEE Circuits and Devices Magazine*, **21**, 16-26 (2005).

[5] R. Carter *et al.*, 22nm FDSOI technology for emerging mobile, Internet-of-Things, and RF applications, *Electron Devices Meeting (IEDM), 2016 IEEE International*, 2-2 (2016).

[6] T. Yamada *et al.*, Suppression of drain-induced barrier lowering in silicon-on-insulator MOSFETs through source/drain engineering for low-operating-power system-on-chip applications, *IEEE Trans Electron Devices*, **60**, 260–267 (2013b).

[7] N. A. Srivastava *et al.,* Analytical modelling of surface potential of modified source FD-SOI MOSFET, *International conference on emerging trends in communication technologies (ETCT),* 1–4 (2016).

[8] S. Tripathi, V. K. Mishra and R. K. Chauhan, Performance Analysis of Dual Metal Gate Modified Source Fully Depleted SOI MOSFET, *i-Manager's Journal on Embedded Systems,* **5**, 7 (2016).

[9] K. P. Pradhan *et al.*, Impact of high-k gate dielectric on analog and RF performance of nanoscale DG-MOSFET, *Microelectronics journal*, **45**, 144-151 (2014).

[10] D. Flandre *et al.*, Fully-depleted SOI CMOS technology for low-voltage low-power mixed digital/analog/microwave circuits, *Analog Integrated Circuits and Signal Processing,* **21**, 213-228 (1999).

[11] B. Razavi, CMOS technology characterization for analog and RF design, *IEEE Journal of Solid-State Circuits,* **34**, 268-276 (1999).

[12] V. Kilchytska *et al.*, Influence of device engineering on the analog and RF performances of SOI MOSFETs, *IEEE Transactions on Electron Devices*, **50**, 577-588 (2003).
[13] N. Mohankumar, B. Syamal and C. K. Sarkar, Influence of channel and gate engineering on the analog and RF performance of DG MOSFETs, *IEEE transactions on Electron Devices,* **57**, 820-826 (2010).
[14] A. Sarkar *et al*., Effect of gate engineering in double-gate MOSFETs for analog/RF applications, *Microelectronics Journal*, **43**, 873-882 (2012).
[15] R. K. Sharma and M. Bucher, Device design engineering for optimum analog/RF performance of nanoscale DG MOSFETs, *IEEE Transactions on Nanotechnology*, **11**, 992-998 (2012).
[16] J. P. Colinge, Fully-depleted SOI CMOS for analog applications, *IEEE Transactions on Electron Devices*, **45**, 1010-1016 (1998).
[17] R. K. Chauhan and V. K. Mishra, Area efficient layout design of CMOS circuit for high-density ICs, International Journal of Electronics., **105**, 73-87 (2017).
[18] M. Bhoir *et al.*, Impact of substrate on the frequency behavior of trans-conductance in ultrathin body and BOX FDSOI MOS devices-a physical insight, *VLSI Technology, Systems and Application (VLSI-TSA), 2017 International Symposium on*. IEEE, 1-2 (2017).
[19] H. Yadav and R. K. Chauhan, Performance Scrutiny of Source and Drain Engineered Dual-Material Double-Gate (DMDG) SOI MOSFET with Various High-k, *in 6th International Conference on Frontiers of Intelligent Computing: Theory and Applications (FICTA)*, 533-539 (2017).
[20] H. Yadav and R. K. Chauhan, Novel Technique of Source and Drain Engineering for Dual-Material Double-Gate (DMDG) SOI MOSFETs, *International Conference on Electrical, Electronics, Materials and Applied Science*, 276-281 (2017).
[21] N. Yadava and R. K. Chauhan, Analysis of N+N- Epi-Source Asymmetric Double Gate FD-SOI MOSFET, *Frontiers of Intelligent Computing: Theory and Applications (FICTA), Bhubaneswar*, India, 541-549 (2017).
[22] A. K. Malviya and R. K. Chauhan, Analysis of Source/Drain Engineered 22nm FDSOI using High-k Spacers, International *Conference on Electrical, Electronics, Materials and Applied Science (ICEEMAS)*, Secunderabad, India., 1-6 (2017).
[23] A. K. Malviya and R. K. Chauhan, Optimizing performance of dual metal gate modified source FDSOI using symmetric and asymmetric oxide spacers, *International Conference on Emerging Trends in Computing and Communication Technologies (ICETCCT)*, Dehradun, India., 1-4 (2017).
[24] W. M. Arden, The international technology roadmap for semiconductors—perspectives and challenges for the next 15 years, *Current Opinion in Solid State and Materials Science*, **6**, 371-377 (2002).
[25] S. M. Sze and K. K. Ng, Physics of Semiconductor Devices, *third ed., John Wiley and Sons*, New Jersey, USA, 2009.