An Optimization Algorithm of Variable Allocation Based on Block Architecture

XU Chao1,2, HE Yan-xiang1,3, CHEN Yong1,3, WU Wei1,3, Zeng Xiao-ling1,3

1 School of computer of Wuhan University, Wuhan 430072 P. R. China
2 Xuzhou College of Industrial Technology, Jiangsu, Xuzhou 221000, China
3 State Key Laboratory of Software Engineering of Wuhan University, Wuhan 430072 P. R. China

Received: 13 Oct. 2012; Revised 2 Nov. 2012; Accepted 16 Nov. 2012
Published online: 1 Mar. 2013

Abstract: In this paper, an optimization algorithm of selection block instruction (heuristic allocation algorithm) based on 8-bit microprocessor of block memory architecture as experiment platform is proposed to solve the problem of variable allocation and reduce the number of selection instructions. First the RAM space allocation is designed in an optimizational way, then an heuristic allocation algorithm of variable is designed, finally the position inserted by selection block instructions is optimized. This method can reduce the number of selection block instructions effectively and produce a good effect in code compression. To verify the correctness and efficiency of the above algorithm, this paper adopts the actual embedded system as test case to perform in the experiment. The result shows that the method can obviously reduce the number of selection block instructions, save memory space and improve the integral performance of system.

Keywords: 8-bit microprocessor, block architecture, variable allocation, optimization of selection block instruction

1. Introduction

When embedded system is developed, memory space and computing power in target platform is limited, the general compilation tool chain requires large memory and strong computing power, so it is impossible to compile in the same computer. Embedded cross-compiler[13] which can compile executable code for target platform in host platform with strong CPU and enough space is introduced to solve the problem. By contrast with universal system, embedded system puts forward more requirements on cost, power consumption and function for quality of application software. Since cost of ic chip is in proportion to area density of that, the density is higher, the capacity is larger and the cost will be higher. If code generated by embedded compiler isn’t optimized fully[3], it is likely to upgrade hardware system and push business cost. So code quantity in embedded system[7] can have immediate impact on hardware cost. In the process of embedded system development, it is crucial to optimize code[4][15]. Only when is code size reduced as far as possible, system efficiency can be improved.

8-bit microprocessor[8] is most widely used accounting for 55% in the embedded platform field. Usually the space of memory address supported by 8-bit microprocessor is limited. 8-bit microprocessor usually adopts block architecture and combines corresponding selection block instructions to access the data space beyond single block for expanding the limited memory space[10]. The selection block instructions can be inserted into source code to select the block the next instruction will reach, but the insertion can increase code size and the cost of execution time[2]. Therefore, how to insert selection block instructions as less as possible is meaningful for embedded platform with limited space. This paper takes 8-bit microprocessor with block architecture as platform, expects to reduce the number of awaiting selection block instructions by analyzing relationship between variables in program beginning with variable allocation to realize better code optimization.

To begin with, the paper introduces a prerequisite of knowledge. In Section 2 block architecture of 8-bit microprocessor is introduced. In Section 3 an heuristic allocation algorithm for variable is introduced including the optimum
design of RAM space allocation and insertion position of selection block instructions. In Section 4 results and analysis are demonstrated. In the last part related work and conclusion are presented.

2. An Introduction to 8-bit Microprocessor Platform

In this paper 8-bit microprocessor of HR6P series adopting RISC Harvard structure is embedded with hardware multiplier and encrypted by special users’ code, the instruction of which has the characteristics of high confidentiality and efficiency. Buses of program and data access in the structure are mutually independent. Chip instruction set in this series has 48 reduced instructions in it with the characteristics of high coding efficiency and easy extension. Chip integrates many devices including PWM, analog comparing, LCD DRIVER, communication module, program memory with capacity from 2K16bits to 8K16bits, data memory with capacity from 1288bits to 1K8bits and so on. HR6F series chip is given as an example demonstrating the structure diagram in Figure 1.

3. The Design of Optimization Algorithm of Selection Block Instructions

Block architecture only supports serial data access, which means CPU only can access data space in one block once and which block will be accessed depends on the specific selection block instruction. Usually CPU has a special register to store the address of the selection instruction. By inserting the selection instruction into source code the block that the next instruction will reach will be selected. But the insertion of the selection instruction increases code size and pushes the cost of execution time. So how to insert selection instruction as less as possible is meaningful for the embedded platform with limited space.

3.1. The Optimum Design of RAM Space Allocation

Optimization for RAM space allocation is that life period of each local variable is achieved by analyzing control flow and data flow of function and non-life-period-overlap variable can be allocated in same RAM space without influencing the correctness of program. Optimization Algorithm 1 for RAM space allocation is shown as follows:

**Algorithm 1**

**Input:**
three address code statements before optimization

**Output:**
three address code statements after optimization

1. Analyze control flow and data flow and generate ud chain of local variable in function
2. Achieve life period of each variable according to ud chain
3. Calculate life period overlap of each variable to get overlap graph
4. Allocate variable according to overlap graph

To illustrate optimization algorithm for RAM space allocation, a specific function shown in Figure 2 is taken as an example and the concrete implementation procedure is presented.

In Figure 2, (1) to (8) represents life period of variable. Analyze control flow and data flow in function to get ud chain of function and b represents basic block. Division of life period is shown as follows:
There is neither def nor use in b, b is in life period.

There is no def but use in b if there is a covered block subsequently b is in life period otherwise from the beginning of the block to the last point of use in block is in life period.

There is def but no use in b from the definition point to the finishing of the block is in life period.

Def is before the first point of use if there is a covered block subsequently from the definition point to the finishing of the block is in life period otherwise from the definition point to the last point of use in block is in life period.

Def is between two points of use if there is a covered block subsequently b is in life period otherwise from the beginning of the block to the last point of use in block is in life period.

Def and use are in the same statement b is in life period.

The corresponding space allocation for variable allocation can be achieved from the analysis. For example, a diagram of variable life period and space allocation without optimization is presented in Figure 3.

In Figure 3 life periods of Variable a, b, d, e are achieved by analyzing control flow and data flow and allocated to their respective space. Variable c isn’t analyzed because definition of Variable c isn’t used and is optimized before optimization of space allocation. A space is mapped as a Web, according to the sequence of variable’s definition, space for variable a is short for Web0, space for variable b is short for Web1 and so on. It is shown in Figure 4 that five Webs are respectively allocated to five different variables. The concrete optimization algorithm for space allocation is as follows:

- Calculate the overlap relationship between webs. If two webs’ reachable blocks are not the same, there is no overlap for the two webs. If two webs’ reachable blocks are the same, the statements covered by the two webs in the block should be analyzed. If two webs cover the same statement, it illustrates that they overlap, otherwise they don’t. The overlap relationship between webs is shown in Figure 3.3 in which line represents the overlap between two webs.

- Arrange all webs in order of space size from large to small and then arrange them in order of use frequency from more to less. In this way it can reduce some subsequent chip selection instructions. Store the arranged webs in chained list which is waiting for allocation. Supposing that the size of Web0 in the above diagram is 3, Web1 is 4, Web2 is 1, Web 3 is 2, Web4 is 2, the order of chained list is: web1, web0, web4, web3 and web2.

- Allocate space for web in chained list in turns. Before allocation, judge if this web overlaps the web in the allocated space. If no overlap, this web can be stored in the space and space size depends on the larger one, otherwise space should be allocated again. After web allocation in above diagram the situation is that space size of Web0, Web2 and Web4 is 3, space size of Web1 and Web3 is 4, Web 4 can be put in either of the two spaces for it has no overlap with the two spaces.

3.2. An Heuristic Allocation Algorithm

3.2.1. Brief Introduction to Heuristic Allocation Algorithm of Variable Class

The set in which all of single variable have become several variables after RAM space allocation optimization is allocated to a mutual space. A set is called a variable class. Block architecture of 8-bit microprocessor requires corresponding selection block to access the data space in different block. It means that when variable class can’t be stored in one block after RAM space allocation optimization, how to allocate variable classes to different blocks for reducing the number of selection block instructions should be taken into account.

Two cases are involved: there are two variable classes, if both are in the same block, chip selection instruction
3.2.2. Description of Heuristic Allocation Algorithm of Variable Class

For solving the above problem about variable class allocation, construct an access relationship diagram in which weighted digraph containing node set and edge set is used to describe the variable class access relationship. Each node represents a variable class and weight of node represents space size occupied by variable class; Each edge represents the access relationship between two variable classes and edge weight represents access sequence between two nodes. In this way the access relationship flow diagram can be expressed as $G=(V, E)$. $V$ represents node set or variable class, $E$ represents edge set or access sequence between variable classes. Suppose there are Node $a$ and Node $b$, directed edge $e_{ab}$ represents it accesses Variable $b$ after accessing variable $a$. Construction flow diagram of weighted digraph is presented in Figure 5.

Now a function can explain the construction progress of the above weighted digraph in Figure 6 and 7.

In Figure 7, it is clear that edge weight of Variable $(ab)$ is 2 and edge weight of Variable$(ac)$ and that of Variable $(ad)$ are both 1.

After weighted digraph of variable class access relationship is constructed, heuristic allocation algorithm of variable class becomes the question inserting the least selection block instruction in the weighted digraph. The number of the inserted selection block instruction is influenced by two factors: (1) if two variable classes are in the same block, chip selection instruction isn’t needed. (2) if two variable classes are in different blocks, the neighboring variable classes are allocated to two blocks with less switchover cost. These two factors are the factors of heuristic allocation algorithm. It means that when two variable classes are in the same block, space occupied by variable classes is less than one block, space size occupied is called a heuristic factor; when variable classes are in the different blocks, instruction switchover cost between blocks is another factor, switchover cost is decided by edge weight between blocks and distance between blocks. The concrete description of heuristic allocation algorithm of variable class is shown in Algorithm 2.

Input Variable $G$ as variable class and get an access relationship diagram, where $V$ is variable class, $E$ is access relationship between two variable classes, $V$ and $E$ are parameters of the diagram, input Variable $K$ is the block
3.3. The Optimum Design of Insertion Position of Selection Block Instructions

The above research indicates that variable classes have been allocated to the different blocks in optimization way, therefore, the corresponding selection block instructions need to be inserted into data of access block and the insertion position of instructions will influence the number of insertion instructions which happens between basic blocks. In this paper the optimization of insertion position is divided into two parts: (1) select statements are added to the entries of all basic blocks; (2) find out basic blocks’ joint with bone pattern branches and put the two merged entry selects at the exit of predecessor block to reduce select statements.

Process of algorithm: input a mapping table varsToBank and an intermediate code representation sequence of a function noBSLCodeList to construct basic block of this function (the first line of code); output intermediate code representation sequence inserted selection block instruction; insert corresponding selection block instructions (from line 2 to line 15 of code) in the basic block and then insert selection instruction between basic blocks (from line 16 to line 30 of code); decomposition blocks generates new intermediate code representation sequence BSLCodeList inserted selection block instruction. Function BtoB used to reduce the number of inserted selection block instructions represents the least inserted instructions for block switch over and BtoB(1,2) represents switch over from Block 1 to Block 2. The optimum design of insertion position of selection block instructions in Algorithm 3.

Algorithm 2

Input:
Graph G=(V,E,K)
Output:
V’s K Partition Set P=(P₁,P₂,……,Pₖ)
1: list lst = sort edge weight from large to small
2: while lst is not empty do
3:    if size(u) + size(v) ≤ m then
4:        merge u and v into a vertex set
5:    end if
6:    take out the first two elements in Set(V) to u',v'
7:    for each u ∈ e, v ∈ Set(V) do
8:        f(u,v) = weight(e(u,v)) + distance(u,v)
9:        if f(u,v) < fₘᵢₙ(u',v') then
10:           fₘᵢₙ(u',v') ← f(u,v)
11:           u' ← u
12:           v' ← v
13:    end for
14:    for each a in B do
15:        if varsToBank[a] != currentBank then
16:            varsToBank[a] = currentBank
17:            b.entryBank = varsToBank[a]
18:        end if
19:    end for
20: end while

Algorithm 3

Input:
varsToBank, noBSLCodeList
Output:
BSLCodeList
1: for each b in B do
2:    currentBank = -1;
3:    for each intermediate code i in b do
4:        if i using variable a then
5:            b.entryBank = varsToBank[a]
6:            b.exitBank = currentBank
7:        else if varsToBank[a] != currentBank then
8:            i ← push front(BtoB(currentBank, varsToBank[a]))
9:        end if
10:    currentBank = varsToBank[a]
11: end for
12: end for
13: for each d in b.preBlocks do
14:    if !tmpList.contain(d.exitBank) then
15:        tmpList.add(d.exitBank)
16:    end if
17: end for
18: end for
19: for each d in b in B do
20:    clear tmpList
21:    if tmpList.size == 1 then
22:        b.push front(BtoB(tmpList[0], b.entryBank))
23:    end if
24: end for
25: if tmpList.size > 1 then
26:    b.push front(BtoB(−1, b.entryBank)) //decomposition intermediate code representation sequence
27: end if
28: end for
29: return BSLCodeList
30: end for
31: BSLCodeList = deconstruct the basic blocks B
32: return BSLCodeList
Table 1 The Usage Table of RAM before and after Optimization

<table>
<thead>
<tr>
<th>Test case</th>
<th>RAM after optimization</th>
<th>RAM before optimization</th>
<th>Optimization rate of the algorithm</th>
<th>RAM of PICC</th>
<th>Optimization rate of PICC</th>
</tr>
</thead>
<tbody>
<tr>
<td>ST001</td>
<td>212</td>
<td>297</td>
<td>28.62%</td>
<td>200</td>
<td>32.66%</td>
</tr>
<tr>
<td>ST002</td>
<td>149</td>
<td>203</td>
<td>26.60%</td>
<td>144</td>
<td>29.06%</td>
</tr>
<tr>
<td>ST003</td>
<td>237</td>
<td>326</td>
<td>27.30%</td>
<td>216</td>
<td>33.74%</td>
</tr>
<tr>
<td>ST004</td>
<td>236</td>
<td>341</td>
<td>30.79%</td>
<td>230</td>
<td>32.55%</td>
</tr>
<tr>
<td>ST005</td>
<td>189</td>
<td>258</td>
<td>26.74%</td>
<td>177</td>
<td>31.40%</td>
</tr>
<tr>
<td>ST006</td>
<td>147</td>
<td>199</td>
<td>26.13%</td>
<td>142</td>
<td>28.64%</td>
</tr>
<tr>
<td>ST007</td>
<td>162</td>
<td>218</td>
<td>25.69%</td>
<td>154</td>
<td>29.36%</td>
</tr>
<tr>
<td>ST008</td>
<td>226</td>
<td>312</td>
<td>27.56%</td>
<td>203</td>
<td>34.94%</td>
</tr>
<tr>
<td>T001</td>
<td>120</td>
<td>163</td>
<td>26.38%</td>
<td>114</td>
<td>30.06%</td>
</tr>
<tr>
<td>T002</td>
<td>81</td>
<td>119</td>
<td>31.93%</td>
<td>84</td>
<td>29.41%</td>
</tr>
<tr>
<td>T003</td>
<td>137</td>
<td>189</td>
<td>27.31%</td>
<td>132</td>
<td>30.16%</td>
</tr>
<tr>
<td>T004</td>
<td>97</td>
<td>137</td>
<td>29.20%</td>
<td>94</td>
<td>31.39%</td>
</tr>
<tr>
<td>T005</td>
<td>78</td>
<td>116</td>
<td>32.76%</td>
<td>82</td>
<td>29.31%</td>
</tr>
<tr>
<td>T006</td>
<td>129</td>
<td>184</td>
<td>29.89%</td>
<td>124</td>
<td>32.61%</td>
</tr>
<tr>
<td>T007</td>
<td>118</td>
<td>165</td>
<td>28.48%</td>
<td>115</td>
<td>30.30%</td>
</tr>
<tr>
<td>T008</td>
<td>53</td>
<td>79</td>
<td>32.91%</td>
<td>57</td>
<td>27.85%</td>
</tr>
<tr>
<td>T009</td>
<td>86</td>
<td>123</td>
<td>30.08%</td>
<td>87</td>
<td>29.27%</td>
</tr>
</tbody>
</table>

Table 2 Some HEX File Example

```
:0200000040000FA
:100000000C082B20010826B025824580158055808
:100010025580158065805588A6D005CA06C206471
:10000000038A16CA1640345086CA0662064030862
:1000000026CA06620640308A36C2108A1671510B8
:100040000086CA264846CA0662064030886CA2663D
:10000000038A16CA1640345086CA0662064030862
:0200000008C7A
:020000001FF
```
The optimization effect of the algorithm is better for the small test cases.)

Seen from the comparison among RAM, the number of selection block instructions and ROM space, the optimization algorithm saves the space effectively, reduces the number of selection block instructions obviously, has almost the same optimization effect comparing with the developed industrial compiler PICC but better optimization effect for the small test cases. Since PICC pays more attention to global optimization and adopts uniform allocation, each block has been allocated almost the same number of variables. In this way for the situation with less variables, uniform allocation increases the code cost without good effect of code optimization.

5. Related Work and Conclusion

The optimization algorithm study about variable allocation[1][14][9] has two aspects: concurrent access data and serial access data. In the field of concurrent access data[6], the researchers considered that single instruction can increase the number of block space, and thereby increase memory bandwidth to improve the concurrent execution efficiency of program. In the field of serial access data, the researchers at home and abroad also did some research. In the literature[12][11], Scholz et al in Sydney University proposed an optimization technique that can minimize the cost of block switchover by optimizing the position of insertion block instruction. In the literature Bradlee et al proposed a dynamic programming algorithm on the base of block memory architecture and global shared memory. This method can reduce chip selection instruction by allocating developed PICC but has better optimization effect for some small test cases.)

3.In order to test the influence over the whole system after selection block instruction optimization.size of HEX file (or size of ROM space) generated after each test case optimization is calculated and compared with the developed industrial compiler PICC for assessing effectiveness of optimum design. Comparison of ROM space is shown in Table 4.

(Also, relative optimization rate = ROM after the algorithm optimization/ ROM of PICC. The result in above table shows that space size is almost kept before 0.9-1.1 times of PICC after optimum design, which means its optimization effect is almost the same as that of PICC. Optimization effect of the algorithm is better for the small test cases.)

Table 4 Number Calculation Table of the Inserted Selection Block Instruction before and after Optimization

<table>
<thead>
<tr>
<th>Test case</th>
<th>after optimization instructions</th>
<th>before optimization instructions</th>
<th>Optimization rate of the algorithm</th>
<th>Number of instructions of PICC</th>
<th>Optimization rate of PICC</th>
<th>Optimization rate of the algorithm</th>
</tr>
</thead>
<tbody>
<tr>
<td>ST001</td>
<td>693</td>
<td>950</td>
<td>27.05%</td>
<td>665</td>
<td>30.00%</td>
<td>1.00%</td>
</tr>
<tr>
<td>ST002</td>
<td>192</td>
<td>272</td>
<td>29.41%</td>
<td>201</td>
<td>26.10%</td>
<td>1.01%</td>
</tr>
<tr>
<td>ST003</td>
<td>411</td>
<td>605</td>
<td>32.07%</td>
<td>432</td>
<td>28.60%</td>
<td>0.98%</td>
</tr>
<tr>
<td>ST004</td>
<td>1255</td>
<td>1792</td>
<td>29.97%</td>
<td>1198</td>
<td>33.15%</td>
<td>1.01%</td>
</tr>
<tr>
<td>ST005</td>
<td>879</td>
<td>1210</td>
<td>27.36%</td>
<td>834</td>
<td>31.07%</td>
<td>1.03%</td>
</tr>
<tr>
<td>ST006</td>
<td>1054</td>
<td>1420</td>
<td>25.77%</td>
<td>958</td>
<td>32.54%</td>
<td>0.96%</td>
</tr>
<tr>
<td>ST007</td>
<td>1120</td>
<td>1590</td>
<td>29.56%</td>
<td>1019</td>
<td>35.91%</td>
<td>0.86%</td>
</tr>
<tr>
<td>ST008</td>
<td>332</td>
<td>478</td>
<td>30.54%</td>
<td>348</td>
<td>27.20%</td>
<td>1.06%</td>
</tr>
<tr>
<td>TO01</td>
<td>73</td>
<td>106</td>
<td>31.13%</td>
<td>75</td>
<td>29.25%</td>
<td>1.06%</td>
</tr>
<tr>
<td>TO02</td>
<td>64</td>
<td>95</td>
<td>32.63%</td>
<td>66</td>
<td>30.35%</td>
<td>1.00%</td>
</tr>
<tr>
<td>TO03</td>
<td>108</td>
<td>145</td>
<td>25.52%</td>
<td>99</td>
<td>31.72%</td>
<td>0.92%</td>
</tr>
<tr>
<td>TO04</td>
<td>146</td>
<td>211</td>
<td>30.81%</td>
<td>154</td>
<td>27.01%</td>
<td>1.10%</td>
</tr>
<tr>
<td>TO05</td>
<td>175</td>
<td>243</td>
<td>27.98%</td>
<td>164</td>
<td>32.51%</td>
<td>0.91%</td>
</tr>
<tr>
<td>TO06</td>
<td>26</td>
<td>38</td>
<td>31.58%</td>
<td>27</td>
<td>28.95%</td>
<td>1.04%</td>
</tr>
<tr>
<td>TO07</td>
<td>182</td>
<td>248</td>
<td>26.61%</td>
<td>170</td>
<td>31.45%</td>
<td>1.06%</td>
</tr>
<tr>
<td>TO08</td>
<td>122</td>
<td>162</td>
<td>24.69%</td>
<td>109</td>
<td>32.72%</td>
<td>0.87%</td>
</tr>
<tr>
<td>TO09</td>
<td>98</td>
<td>139</td>
<td>29.50%</td>
<td>101</td>
<td>27.34%</td>
<td></td>
</tr>
</tbody>
</table>

Figure 9 The Corresponding Usage Bar Chart of the Selection Block Instruction before and after Optimization
some frequently switching variables to shared memory. In the literature Minming Li et al in City University of H.K proposed a rounding two approximation algorithm by analyzing CFG[5]. The above methods all suppose that variables have been allocated to each block in advance before optimization of chip selection instruction. But if variables can be allocated automatically to put variables with close relationship to the same block through program in terms of relationship between variables before variables allocation, probably better allocation effect can be achieved to reduce chip selection instruction and programming load of programmer. So this paper studies how to reduce the inserted selection block instructions in terms of variables allocation and combines optimum design of instruction insertion position to achieve better optimization effect.

This paper introduces the block architecture of 8-bit microprocessor, the architecture of HR6P series chip used as experiment platform and instruction system. Next, heuristic allocation algorithm is proposed in the paper when the question of variable allocation is mentioned. At the same time, the detailed algorithms about optimum design of RAM space allocation and selection block instruction are presented. Finally correctness and effectiveness are verified through experiment and the experimental result shows that the design saves the space effectively, reduces the number of selection block instruction obviously and achieves effect of space optimization. In the future work, we’ll try to find better allocation algorithm of variable class and seek the best way to allocate variable class so that the number of selection block instruction will be reduced further. Meanwhile, test case set will be improved to increase the correctness and comprehensiveness of test.

Acknowledgement

The paper is supported by the State Key Program of National Natural Science Foundation of China (Grant No. 91118003), National Natural Science Foundation of China (Grant No. 61170022), Jiangsu Qing Lan Project and Jiangsu Overseas Research Training Program for University Prominent Young Middle-aged Teachers and Presidents.

References

He Yanxiang holds PhD in Computer Science from Wuhan University of Hubei, China. He is Professor of Wuhan University, PhD supervisor, senior member of China Computer Federation, his research interests include trusted software, distributed parallel processing, and software engineering.